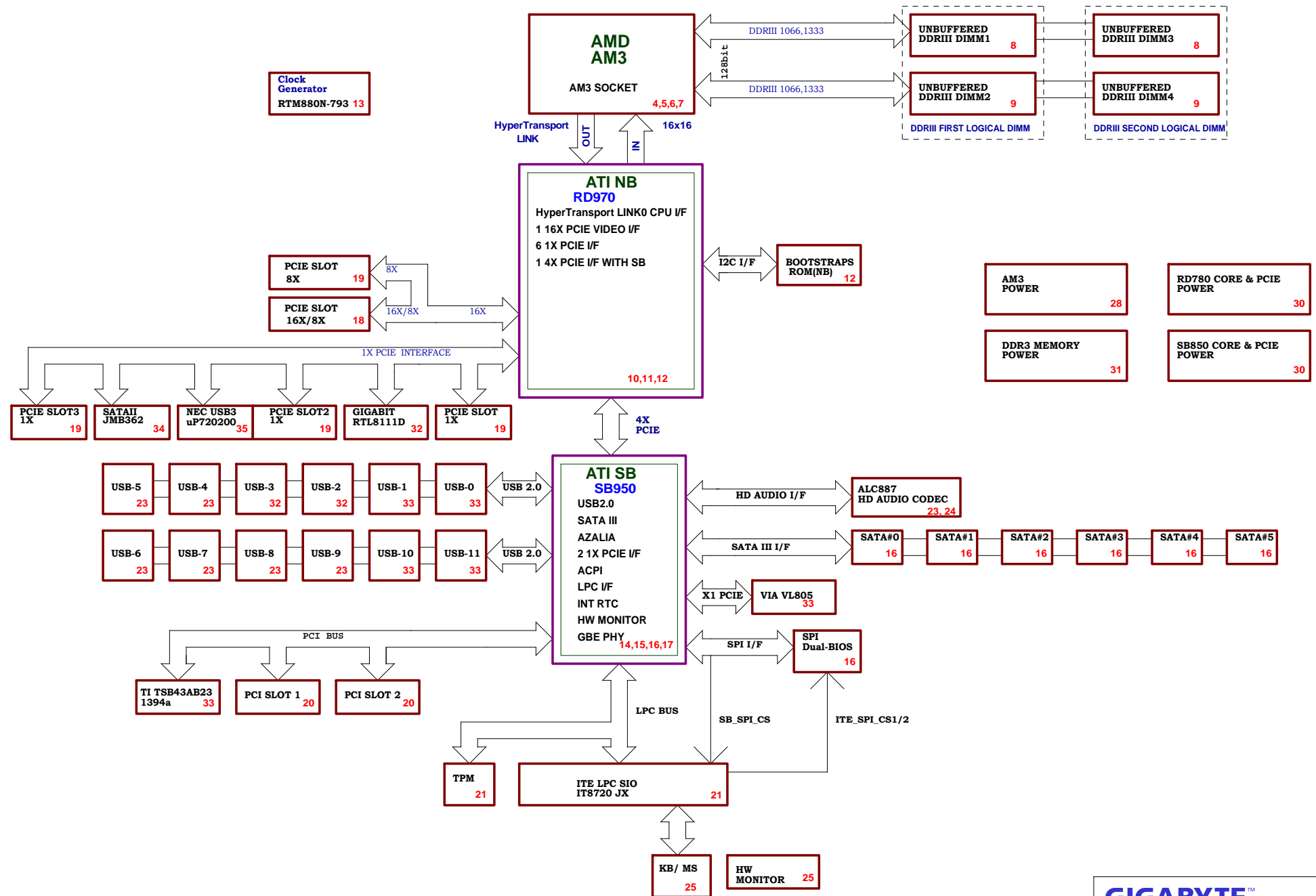


Version: 1.0
P-Code: U98094-0

[illegible]

Circuit or PCB layout change for next version

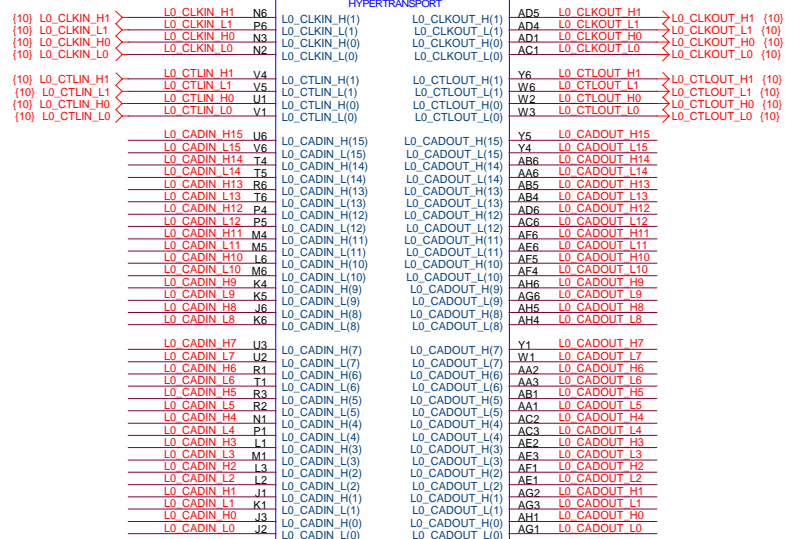
[illegible]



L0_CADIN_L[0..15] < L0_CADIN_L[0..15] (10)
 L0_CADIN_H[0..15] < L0_CADIN_H[0..15] (10)
 L0_CADOUT_L[0..15] < L0_CADOUT_L[0..15] (10)
 L0_CADOUT_H[0..15] < L0_CADOUT_H[0..15] (10)

M2CPUA

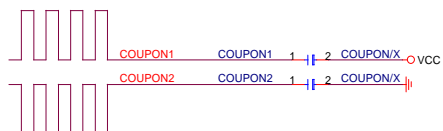
HYPERTRANSPORT



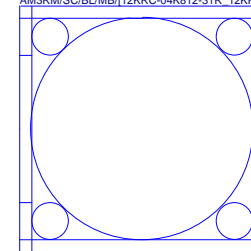
CPU-SK/942AM3b/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

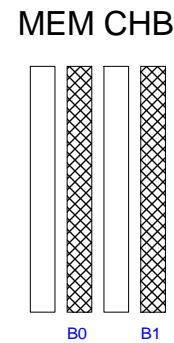
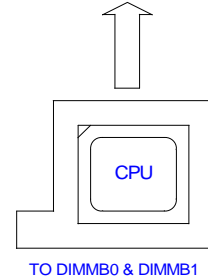
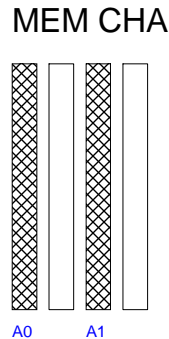
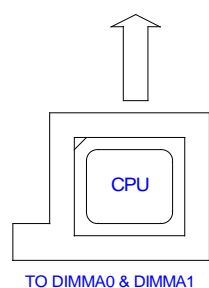
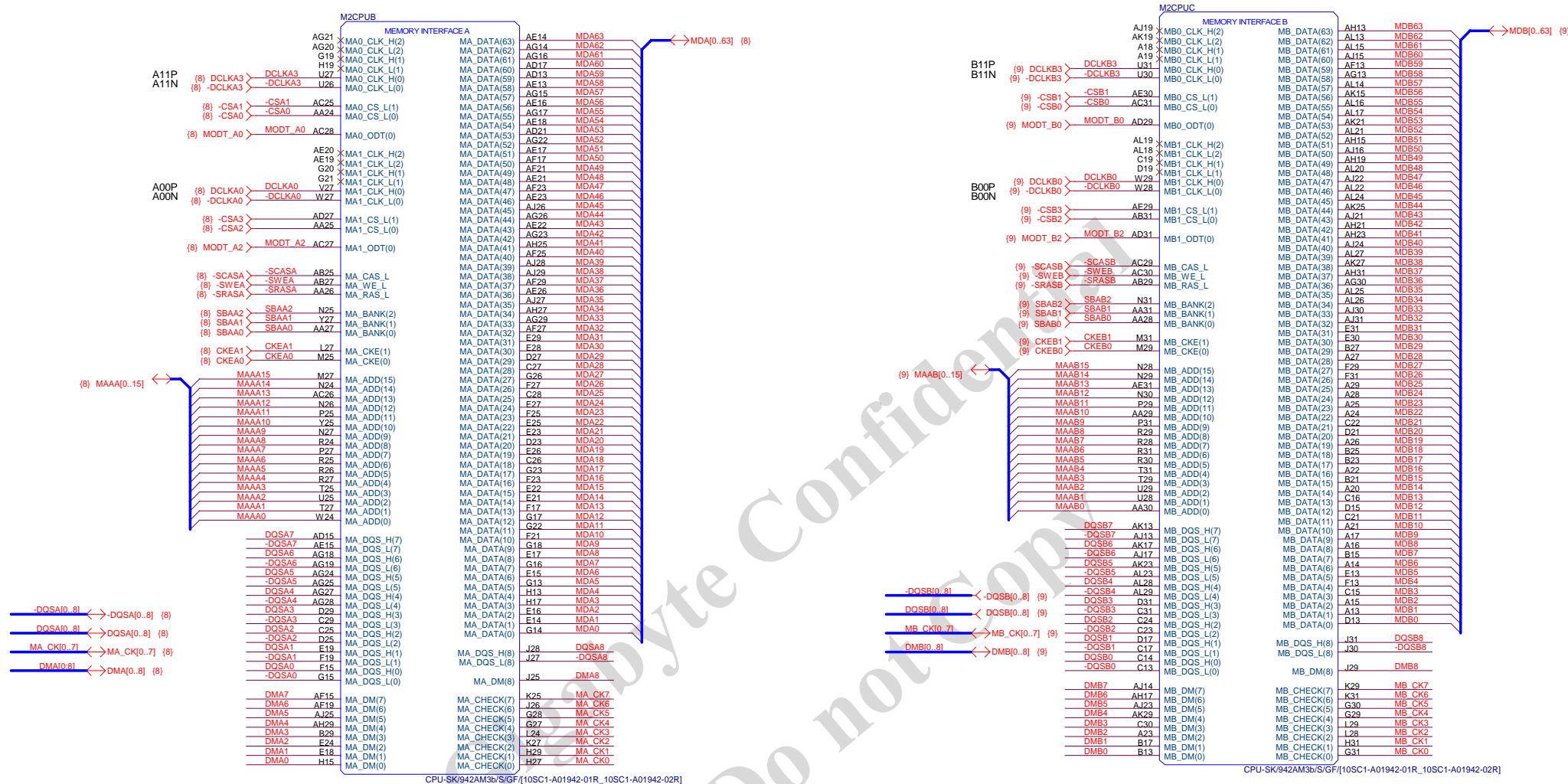
VLDT_A = VCC12_HT
 VLDT_B = HT12B



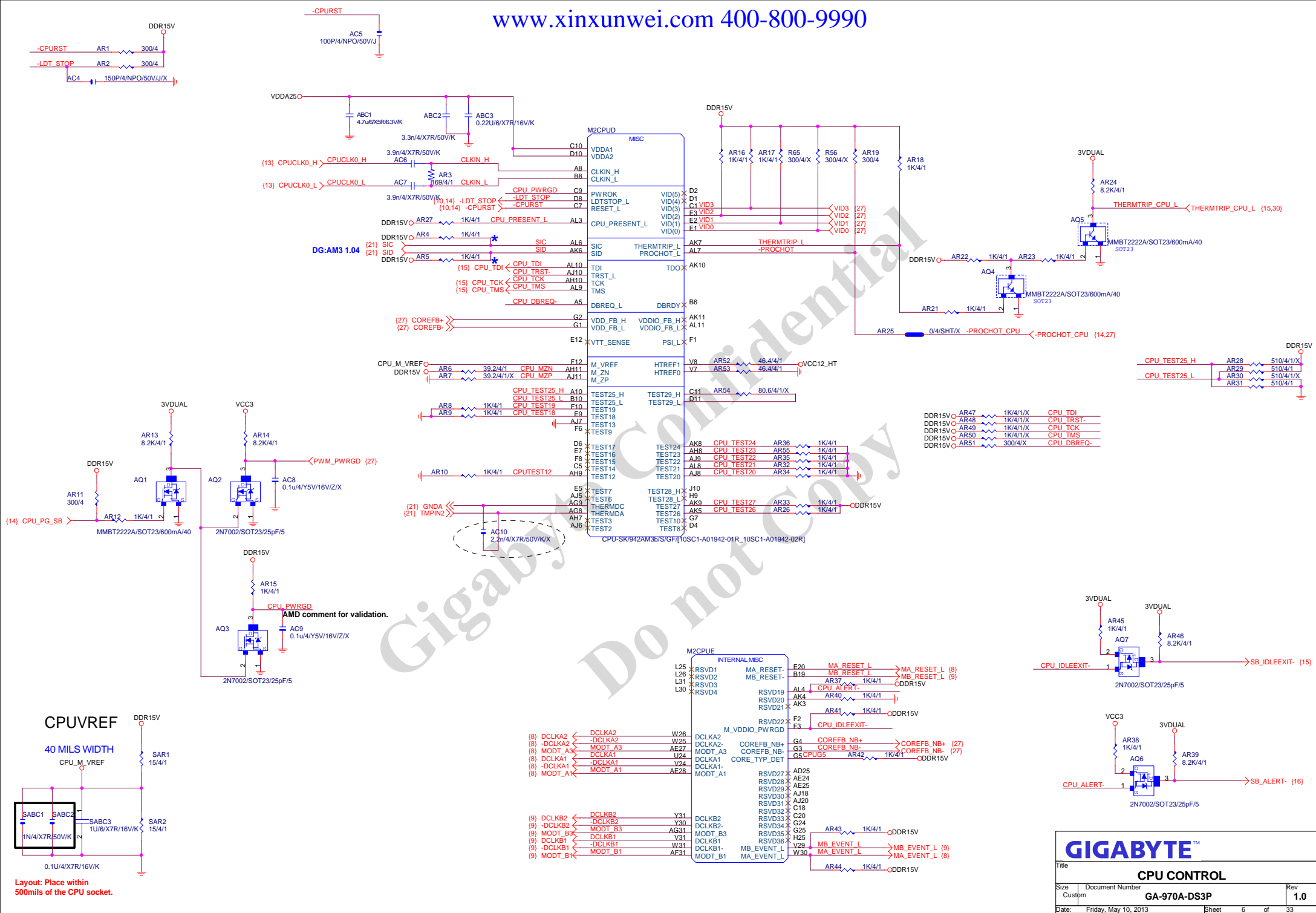
M2CPU
 AM3RM/SC/BL/MB/[12KRC-04K812-31R_12KRC-04K812-32R]

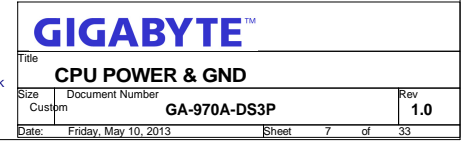


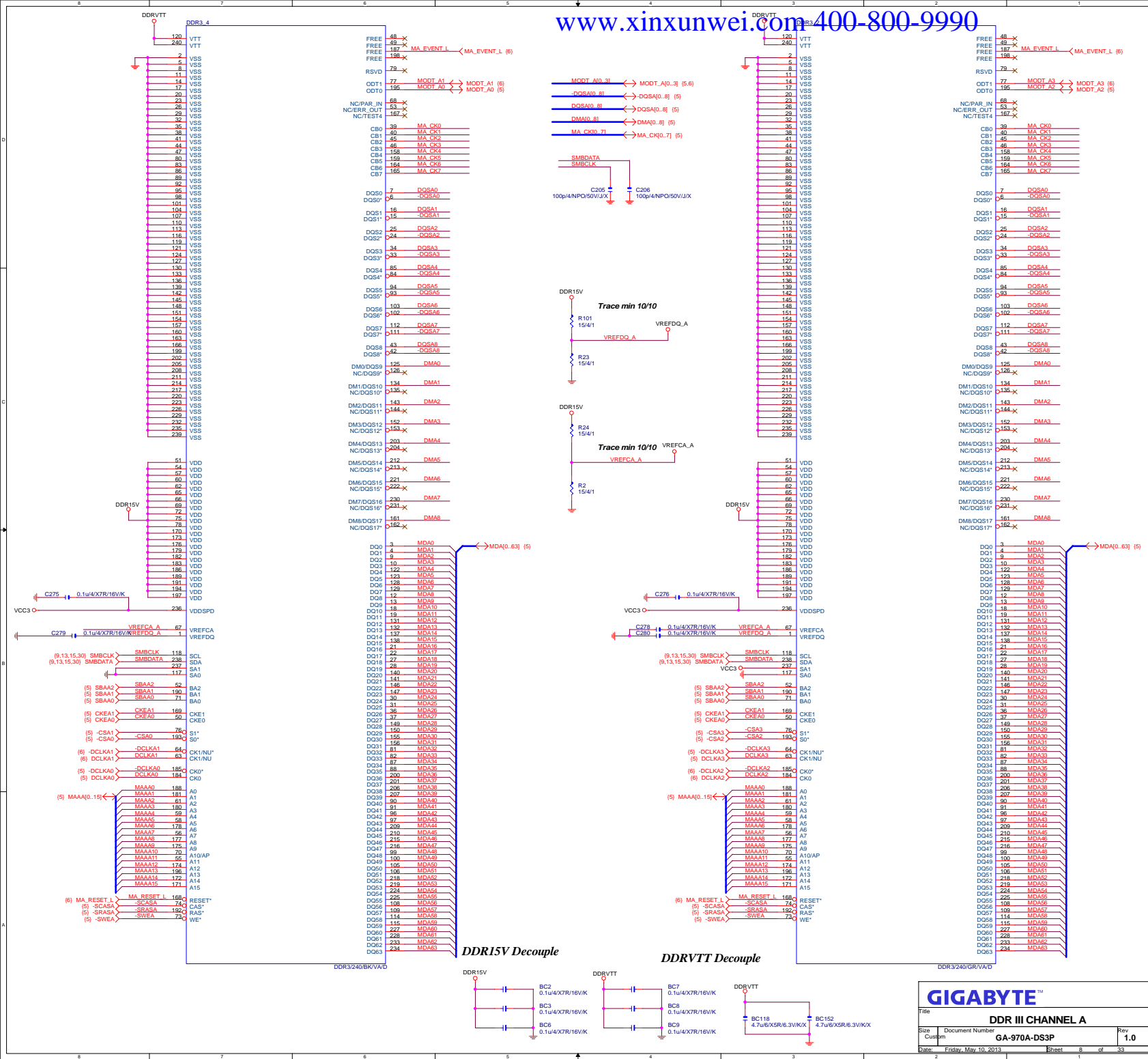
GIGABYTE™			
Title			
CPU HYPER TRANSPORT			
Size	Document Number	Rev	
Custpm	GA-970A-DS3P	1.0	
Date:	Friday, May 10, 2013	Sheet	4 of 33

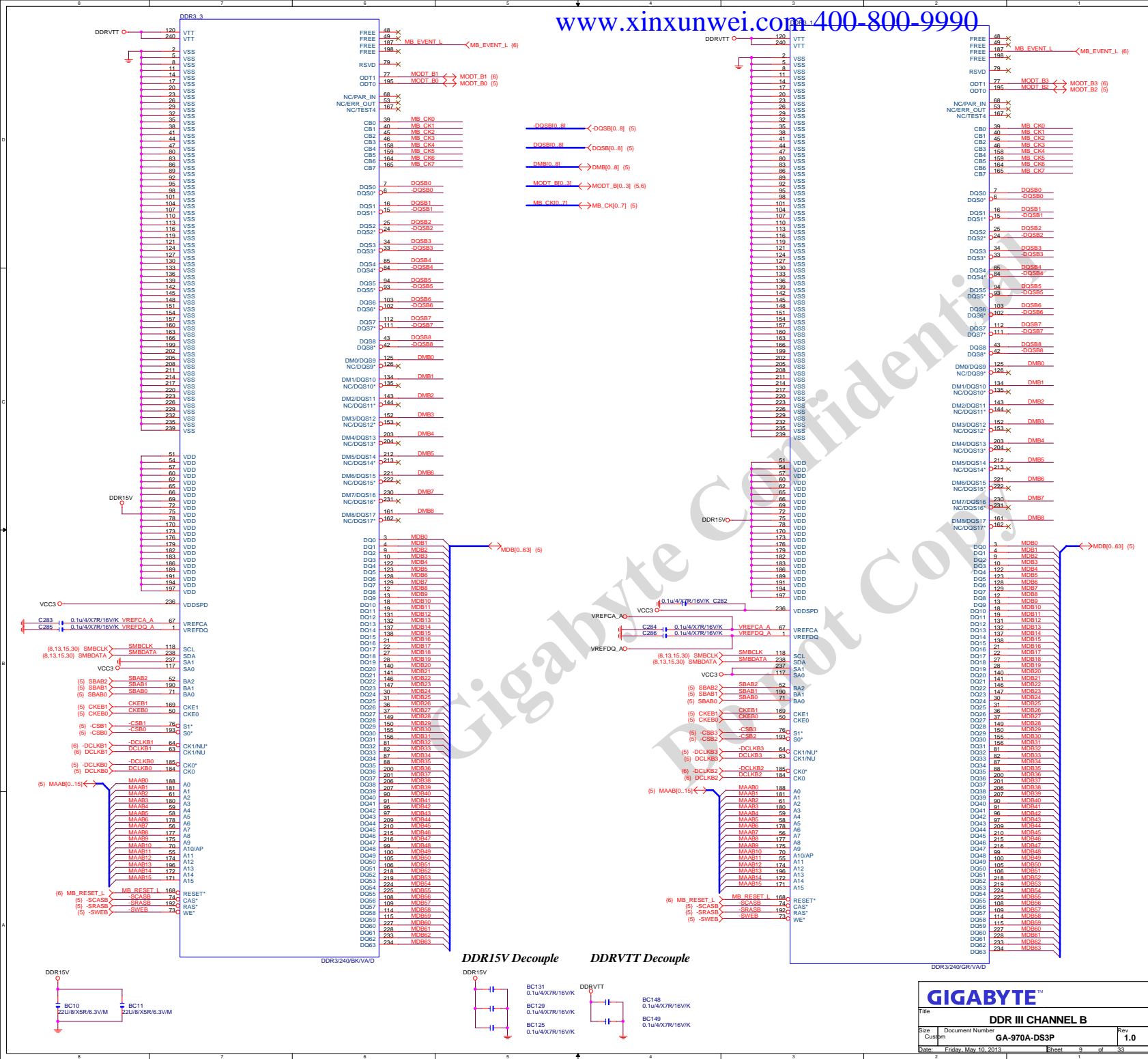


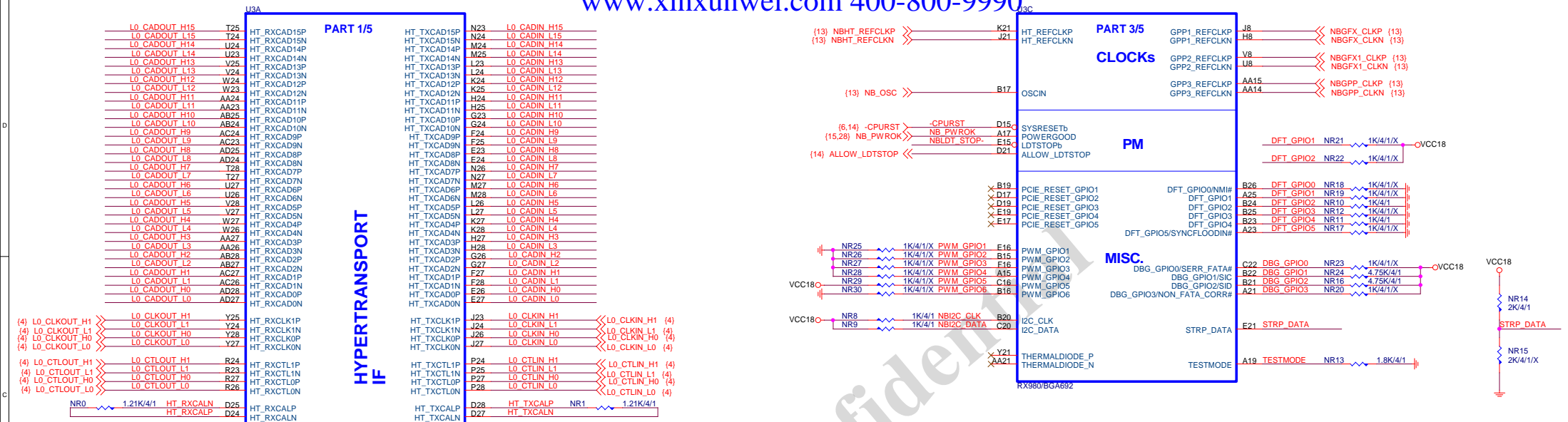
GIGABYTE™			
CPU DDRIII MEMORY			
Title	Document Number		Rev
Size	GA-970A-DS3P		1.0
Custom			
Date:	Friday, May 10, 2013	Sheet	5 of 33













U3B

PART 2/5

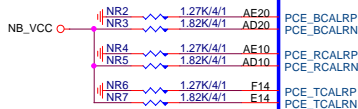
EXP A_RXP15	N6	GPP1_RX15P	GPP1_TX15P	N3	EXP A_TXP15
EXP A_RXN15	N5	GPP1_RX15N	GPP1_TX15N	M2	EXP A_TXN15
EXP A_RXP14	M5	GPP1_RX14P	GPP1_TX14P	M1	EXP A_TXN14
EXP A_RXN14	M4	GPP1_RX14N	GPP1_TX14N	L3	EXP A_TXP13
EXP A_RXP13	L6	GPP1_RX13P	GPP1_TX13P	L2	EXP A_TXN13
EXP A_RXN13	L5	GPP1_RX13N	GPP1_TX13N	K2	EXP A_TXP12
EXP A_RXP12	K5	GPP1_RX12P	GPP1_TX12P	K1	EXP A_TXN12
EXP A_RXN12	K4	GPP1_RX12N	GPP1_TX12N	J3	EXP A_TXP11
EXP A_RXP11	J6	GPP1_RX11P	GPP1_TX11P	J2	EXP A_TXN11
EXP A_RXN11	J5	GPP1_RX11N	GPP1_TX11N	H2	EXP A_TXP10
EXP A_RXP10	H5	GPP1_RX10P	GPP1_TX10P	H1	EXP A_TXN10
EXP A_RXN10	H4	GPP1_RX10N	GPP1_TX10N	G3	EXP A_TXP9
EXP A_RXP9	G6	GPP1_RX9P	GPP1_TX9P	G2	EXP A_TXN9
EXP A_RXN9	G5	GPP1_RX9N	GPP1_TX9N	F2	EXP A_TXP8
EXP A_RXP8	F5	GPP1_RX8P	GPP1_TX8P	F1	EXP A_TXN8
EXP A_RXN8	F4	GPP1_RX8N	GPP1_TX8N	E3	EXP A_TXP7
EXP A_RXP7	D2	GPP1_RX7P	GPP1_TX7P	E2	EXP A_TXN7
EXP A_RXN7	D1	GPP1_RX7N	GPP1_TX7N	A4	EXP A_TXP6
EXP A_RXP6	B5	GPP1_RX6P	GPP1_TX6P	B4	EXP A_TXN6
EXP A_RXN6	C6	GPP1_RX6N	GPP1_TX6N	A6	EXP A_TXP5
EXP A_RXP5	D6	GPP1_RX5P	GPP1_TX5P	B6	EXP A_TXN5
EXP A_RXN5	E6	GPP1_RX5N	GPP1_TX5N	B7	EXP A_TXP4
EXP A_RXP4	E7	GPP1_RX4P	GPP1_TX4P	C7	EXP A_TXN4
EXP A_RXN4	F7	GPP1_RX4N	GPP1_TX4N	A8	EXP A_TXP3
EXP A_RXP3	D8	GPP1_RX3P	GPP1_TX3P	B8	EXP A_TXN3
EXP A_RXN3	E8	GPP1_RX3N	GPP1_TX3N	B9	EXP A_TXP2
EXP A_RXP2	E9	GPP1_RX2P	GPP1_TX2P	C9	EXP A_TXN2
EXP A_RXN2	F9	GPP1_RX2N	GPP1_TX2N	A10	EXP A_TXP1
EXP A_RXP1	D10	GPP1_RX1P	GPP1_TX1P	B10	EXP A_TXN1
EXP A_RXN1	E10	GPP1_RX1N	GPP1_TX1N	B11	EXP A_TXP0
EXP A_RXP0	E11	GPP1_RX0P	GPP1_TX0P	C11	EXP A_TXN0
EXP A_RXN0	F11	GPP1_RX0N	GPP1_TX0N		

AC9	GPP2_RX15P	GPP2_TX15P	AF9
AD9	GPP2_RX15N	GPP2_TX15N	AG9
AE8	GPP2_RX14P	GPP2_TX14P	AG8
AE7	GPP2_RX14N	GPP2_TX14N	AH8
AC7	GPP2_RX13P	GPP2_TX13P	AF7
AD7	GPP2_RX13N	GPP2_TX13N	AG7
AE6	GPP2_RX12P	GPP2_TX12P	AG6
AE5	GPP2_RX12N	GPP2_TX12N	AH6
AG5	GPP2_RX11P	GPP2_TX11P	AG4
AF2	GPP2_RX10P	GPP2_TX10P	AH4
AD2	GPP2_RX10N	GPP2_TX10N	AE3
AD1	GPP2_RX9P	GPP2_TX9P	AE2
AB5	GPP2_RX8P	GPP2_TX8P	AC3
AB4	GPP2_RX8N	GPP2_TX8N	AC2
AA6	GPP2_RX7P	GPP2_TX7P	AB2
AA5	GPP2_RX7N	GPP2_TX7N	AB1
Y5	GPP2_RX6P	GPP2_TX6P	AA3
V4	GPP2_RX6N	GPP2_TX6N	AA2
W5	GPP2_RX5P	GPP2_TX5P	Y2
W6	GPP2_RX5N	GPP2_TX5N	V1
V5	GPP2_RX4P	GPP2_TX4P	W2
V4	GPP2_RX4N	GPP2_TX4N	V2
U6	GPP2_RX3P	GPP2_TX3P	V1
U5	GPP2_RX3N	GPP2_TX3N	U3
T5	GPP2_RX2P	GPP2_TX2P	U2
T4	GPP2_RX2N	GPP2_TX2N	T2
R6	GPP2_RX1P	GPP2_TX1P	T1
R5	GPP2_RX1N	GPP2_TX1N	R3
P5	GPP2_RX0P	GPP2_TX0P	R2
P4	GPP2_RX0N	GPP2_TX0N	P2

AD11	GPP3_RX9P	GPP3_TX9P	AH10
AC11	GPP3_RX9N	GPP3_TX9N	AG10
AE12	GPP3_RX8P	GPP3_TX8P	AG11
AD12	GPP3_RX8N	GPP3_TX8N	AE11
AC13	GPP3_RX7P	GPP3_TX7P	AH12
AE14	GPP3_RX6P	GPP3_TX6P	AG12
AD14	GPP3_RX6N	GPP3_TX6N	AG13
AC15	GPP3_RX5P	GPP3_TX5P	AE13
AE16	GPP3_RX4P	GPP3_TX4P	AH14
AD16	GPP3_RX4N	GPP3_TX4N	AG14
AC17	GPP3_RX3P	GPP3_TX3P	AG15
AE18	GPP3_RX2P	GPP3_TX2P	AE15
AD18	GPP3_RX2N	GPP3_TX2N	AH15
AC19	GPP3_RX1P	GPP3_TX1P	AG17
AH20	GPP3_RX0P	GPP3_TX0P	AG18
AG20	GPP3_RX0N	GPP3_TX0N	AG19

AC21	SB_RX3P	SB_TX3P	AG22
AD21	SB_RX3N	SB_TX3N	AH22
AE22	SB_RX2P	SB_TX2P	AF21
AF25	SB_RX2N	SB_TX2N	AG21
AG25	SB_RX1P	SB_TX1P	AF23
AH26	SB_RX0P	SB_TX0P	AG23
	SB_RX0N	SB_TX0N	AG24

RX980/BGA692



PCI_E slot TX need CAP close to slot side

GPP_TX5P_C	NC4	0.1u/4/X7R/16V/K	PCIE5_OP (19)
GPP_TX5N_C	NC3	0.1u/4/X7R/16V/K	PCIE5_ON (19)
GPP_TX4P_C	NC6	0.1u/4/X7R/16V/K	ML_OP (32)
GPP_TX4N_C	NC5	0.1u/4/X7R/16V/K	ML_ON (32)
GPP_TX2P_C	NC10	0.1u/4/X7R/16V/K	PCIE2_OP (19)
GPP_TX2N_C	NC9	0.1u/4/X7R/16V/K	PCIE2_ON (19)
GPP_TX1P_C	NC20	0.1u/4/X7R/16V/K	PCIE1_OP (19)
GPP_TX1N_C	NC19	0.1u/4/X7R/16V/K	PCIE1_ON (19)
GPP_TX0P_C	NC2	0.1u/4/X7R/16V/K	USB3_OP (33)
GPP_TX0N_C	NC1	0.1u/4/X7R/16V/K	USB3_ON (33)
A_TX3P_C	NC11	0.1u/4/X7R/16V/K	A_TX3P (14)
A_TX3N_C	NC12	0.1u/4/X7R/16V/K	A_TX3N (14)
A_TX2P_C	NC14	0.1u/4/X7R/16V/K	A_TX2P (14)
A_TX2N_C	NC13	0.1u/4/X7R/16V/K	A_TX2N (14)
A_TX1P_C	NC15	0.1u/4/X7R/16V/K	A_TX1P (14)
A_TX1N_C	NC16	0.1u/4/X7R/16V/K	A_TX1N (14)
A_TX0P_C	NC18	0.1u/4/X7R/16V/K	A_TX0P (14)
A_TX0N_C	NC17	0.1u/4/X7R/16V/K	A_TX0N (14)

PLACE THESE CAP CLOSE TO NB.

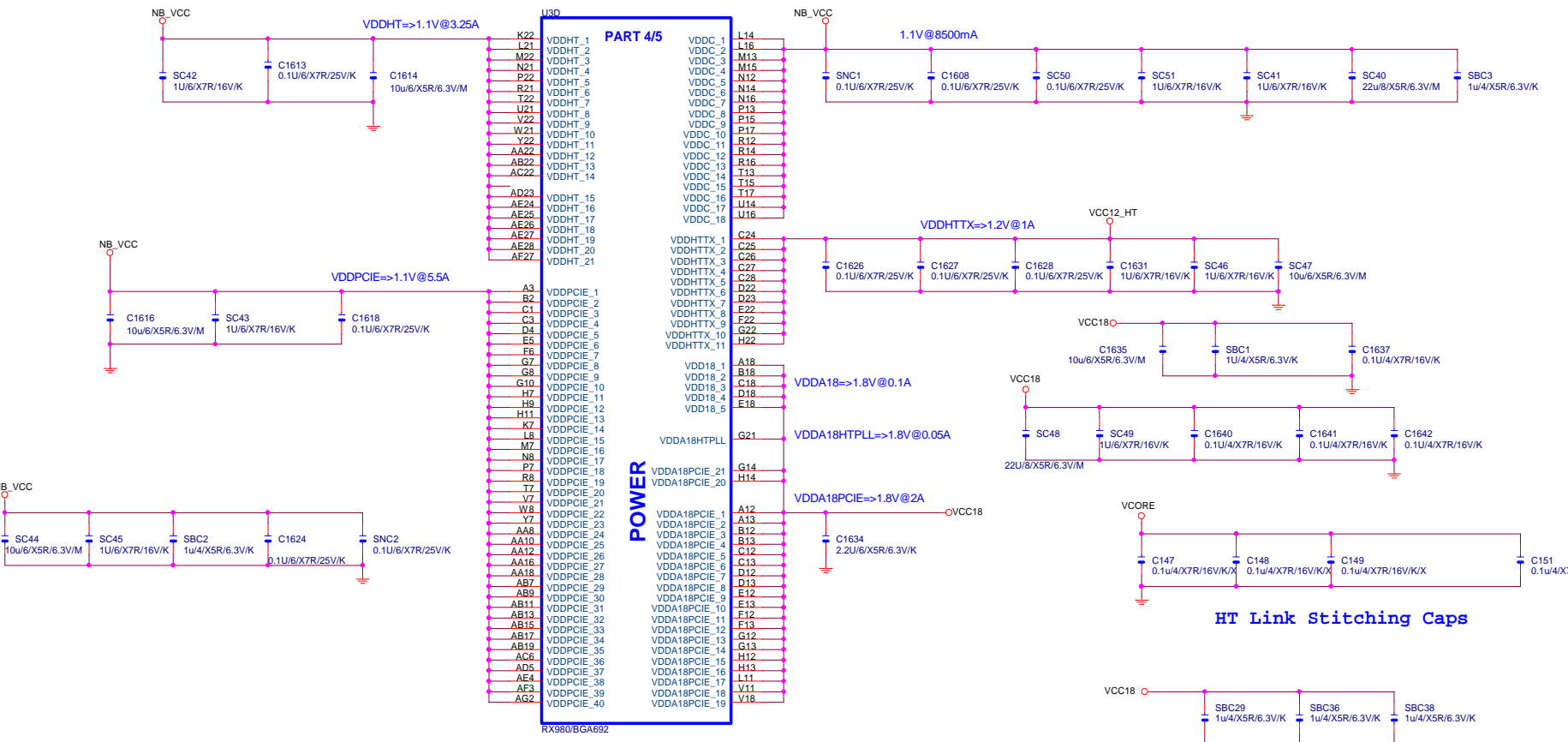
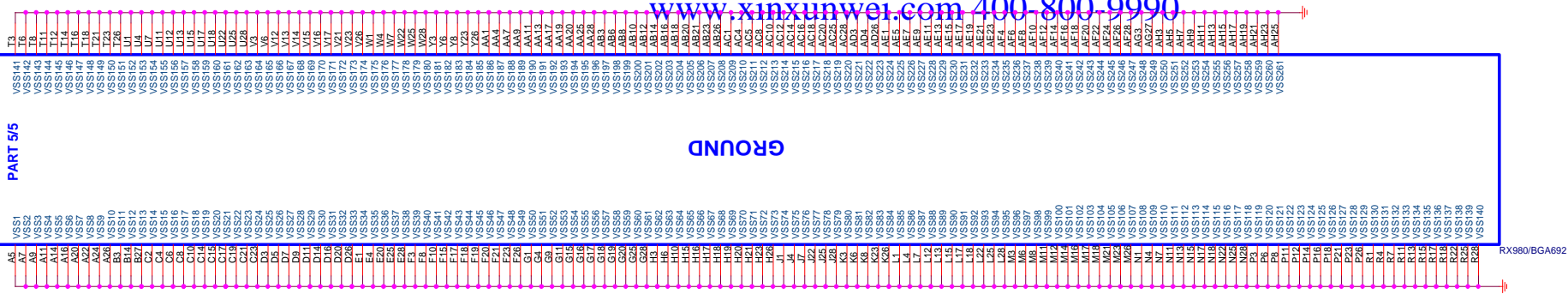
GIGABYTE™

Title
RS780 PCIE I/F ,SwitchSize
Document Number
Custm
GA-970A-DS3PRev
1.0

Date: Friday, May 10, 2013 Sheet 11 of 33

PART 5/5

GROUND



HT Link Stitching Caps

GIGABYTE™

Title
RS780 POWER & GND

Size
Custom

Document Number
GA-970A-DS3P

Rev
1.0

Date: Friday, May 10, 2013

Sheet 12 of 33

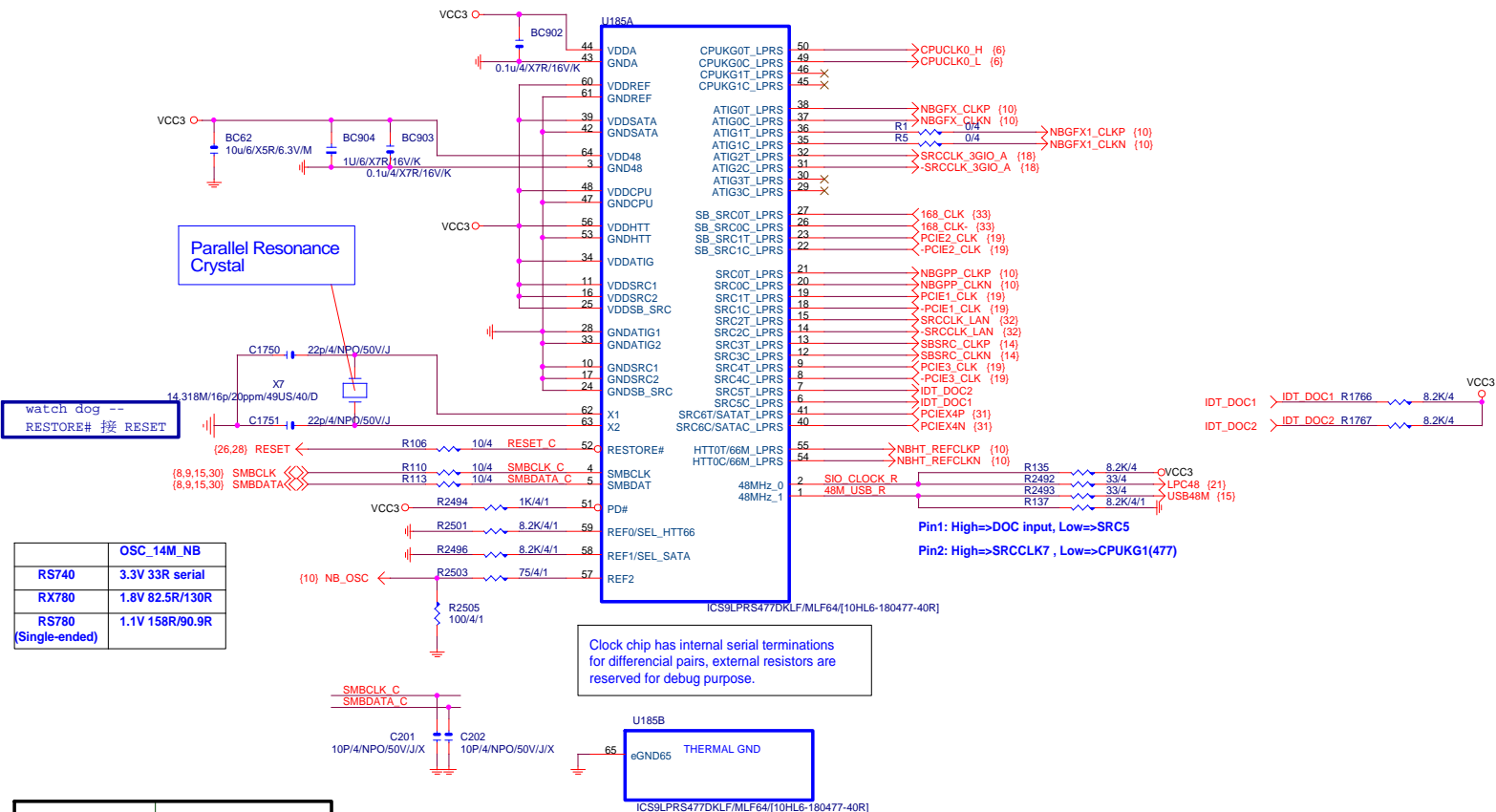
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800
 R851 less than 100 mils away from R800/801
 route CPU clock as 100ohm differential pair



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

GIGABYTE™

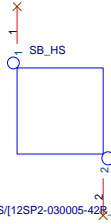
Title RTM880N-793

Size Custom Document Number GA-970A-DS3P Rev 1.0

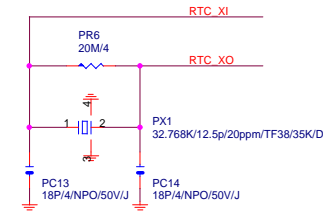
Date: Friday, May 10, 2013 Sheet 13 of 33

 PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

S.B HEATSINK



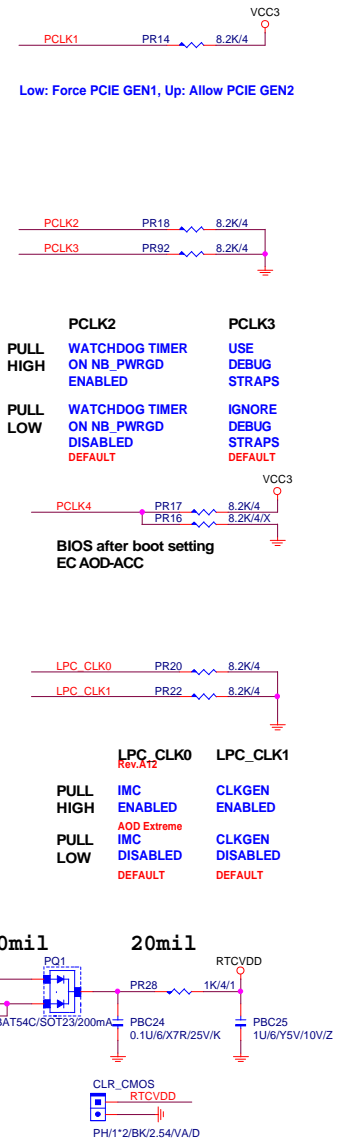
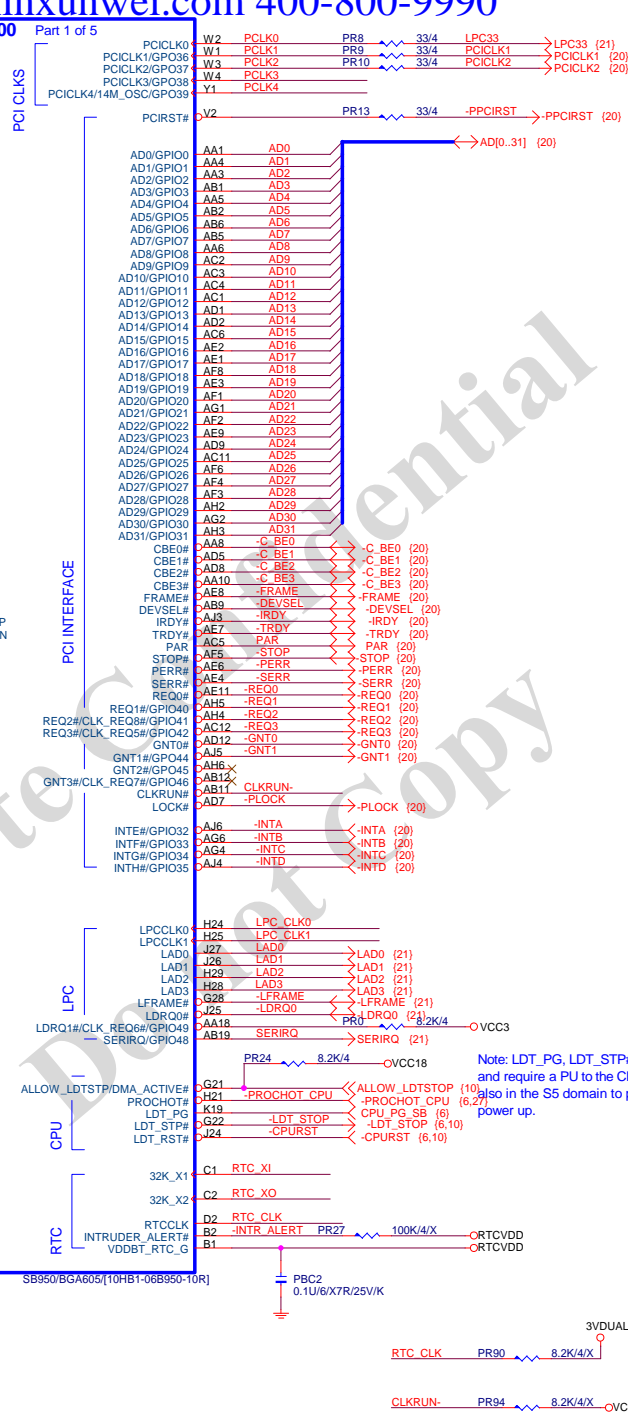
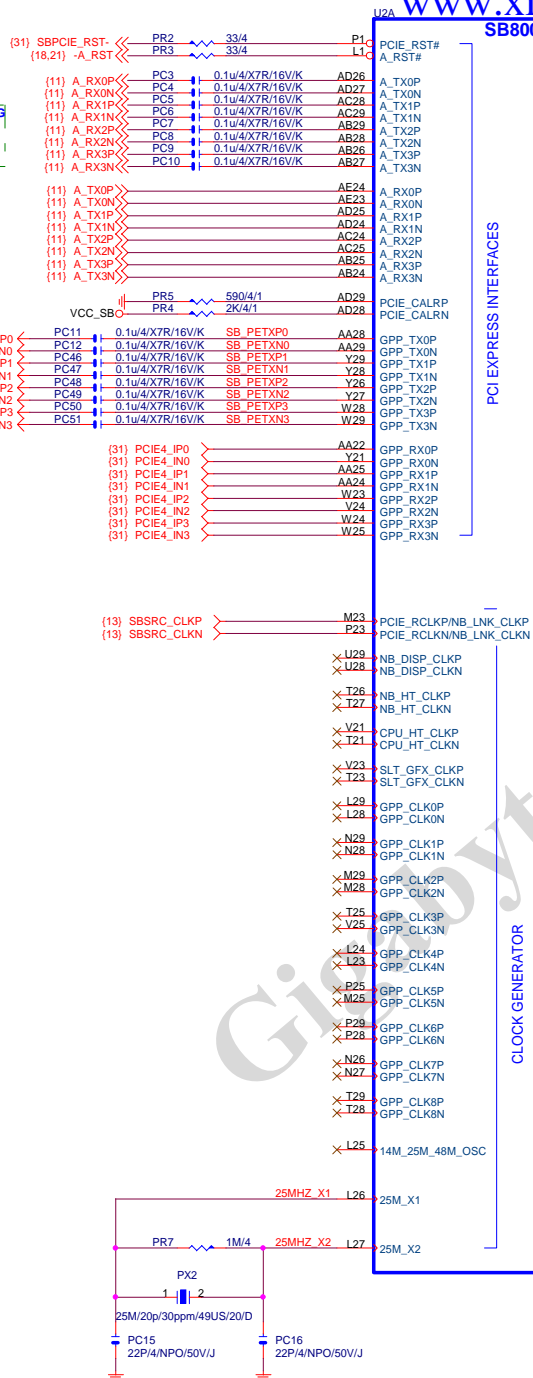
SB_HS/[12SP2-030005-42R_12SP2-030005-43R]



PX1



SHW/D0.64*5.08*6.74

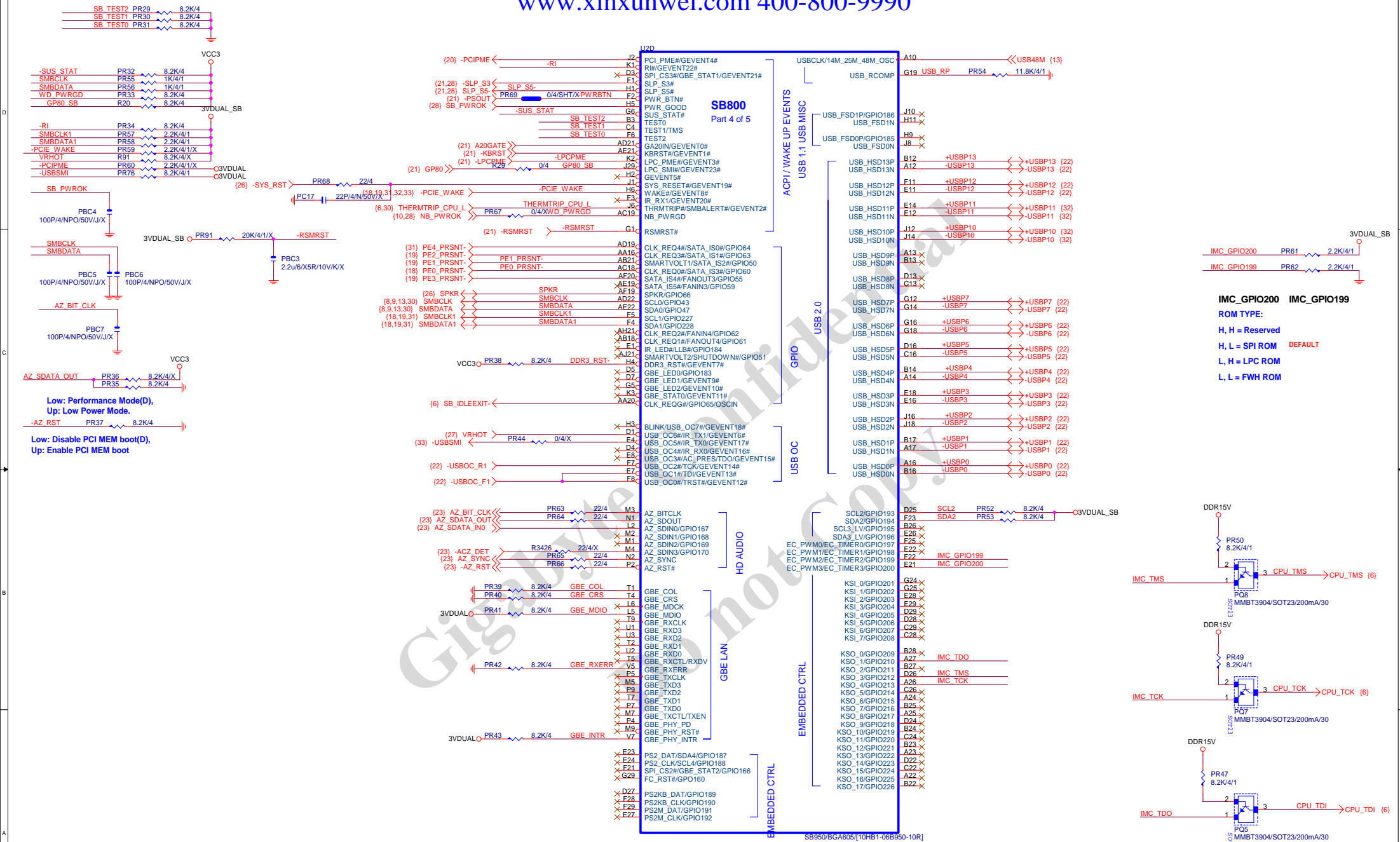


CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

GIGABYTE™

Title			
ATI SB700 PCIE/PCI/CPU/LPC			
Size	Document Number	Rev	
Custom	GA-970A-DS3P	1.0	
Date:	Friday, May 10, 2013	Sheet	14 of 33





PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:

R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

VCC_SB0 PR75 1K/4/1 SATA_CALRP AB14
PR74 931/4/1 SATA_CALRN AA14

(26) -SATA_LED -SATA_LED AD11

TP5 -SATA_X1 AD16

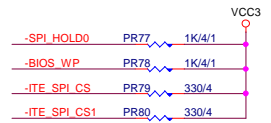
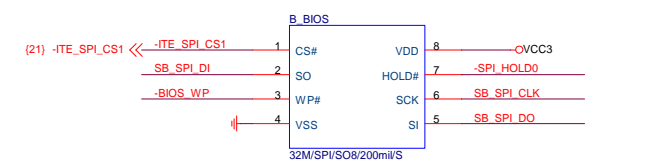
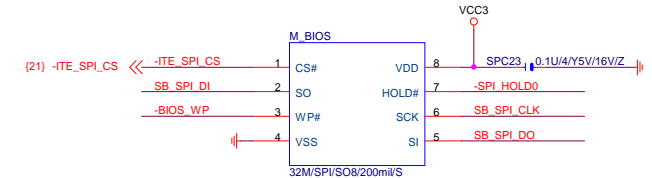
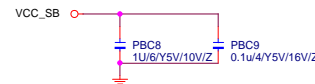
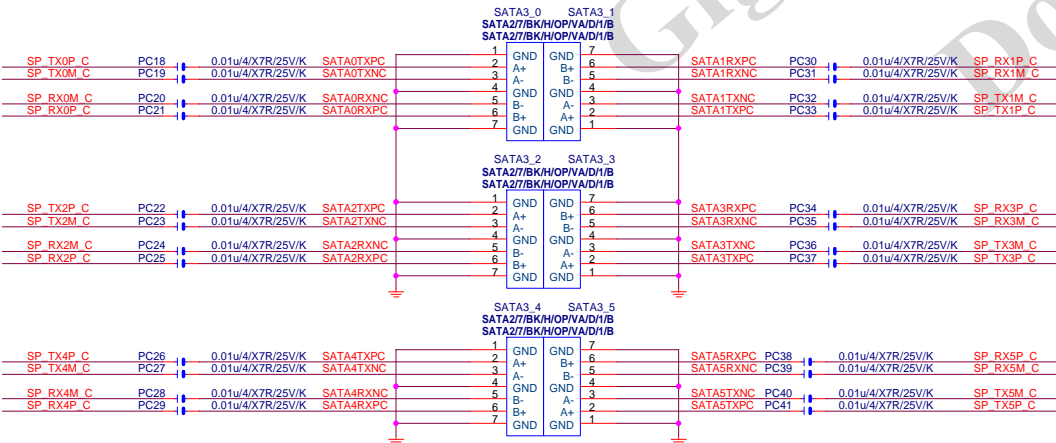
TP7 -SATA_X2 AC16

SB_SPI_DI PR70 22/4 SB_SPI_DI_R J5
SB_SPI_DO PR71 22/4 SB_SPI_DO_R F2
SB_SPI_CLK PR72 22/4 SB_SPI_CLK_R K4
SB_SPI_CS_ITE PR73 22/4 SB_SPI_CS- K9
X G2

SB950/BGA605/[10HB1-06B950-10R]



PLACE SATA AC COUPLING
CAPS CLOSE TO SB850

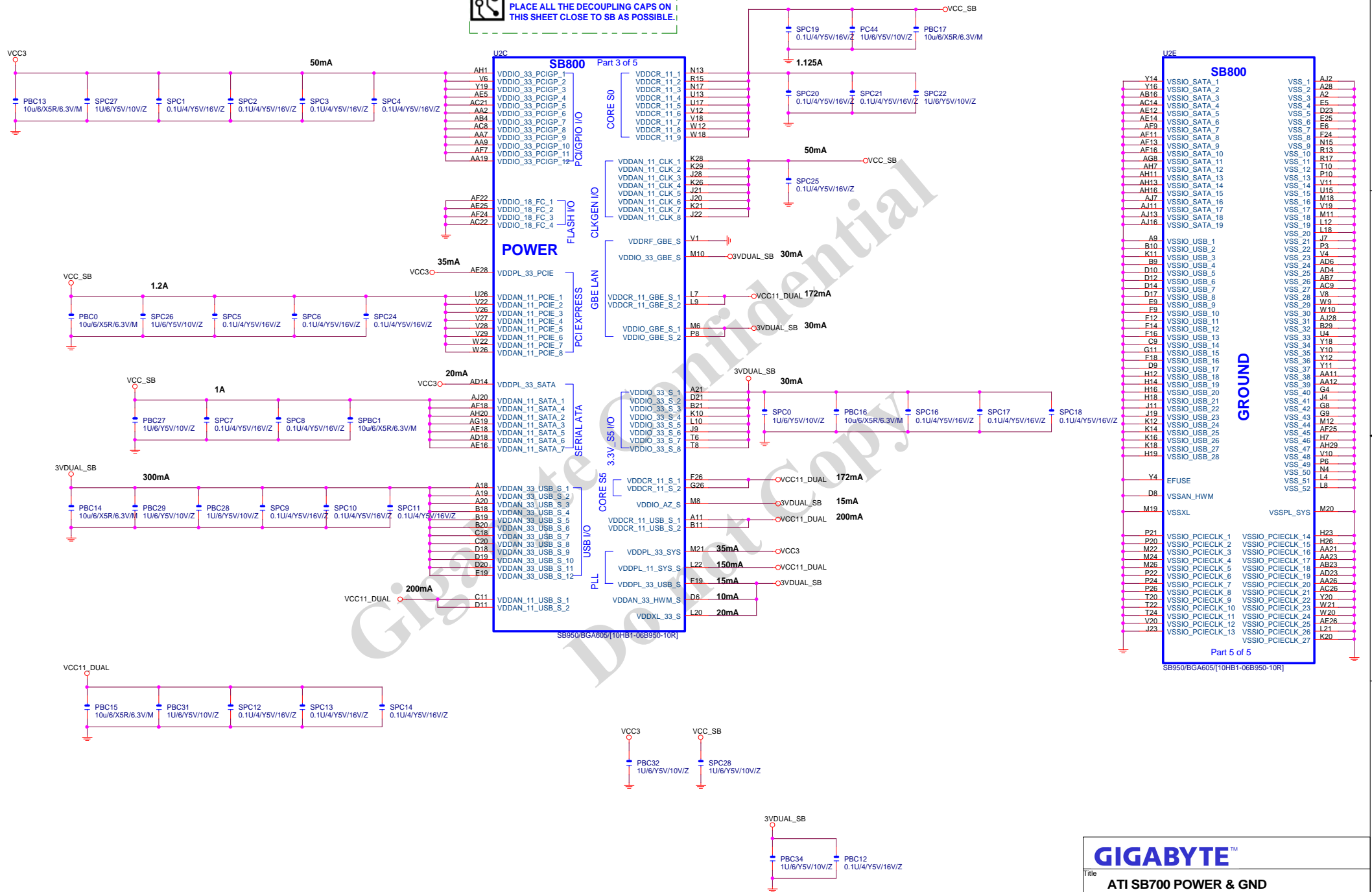


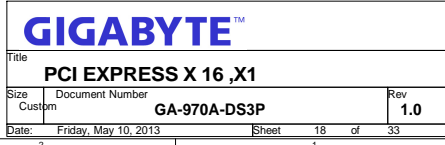
GIGABYTE™

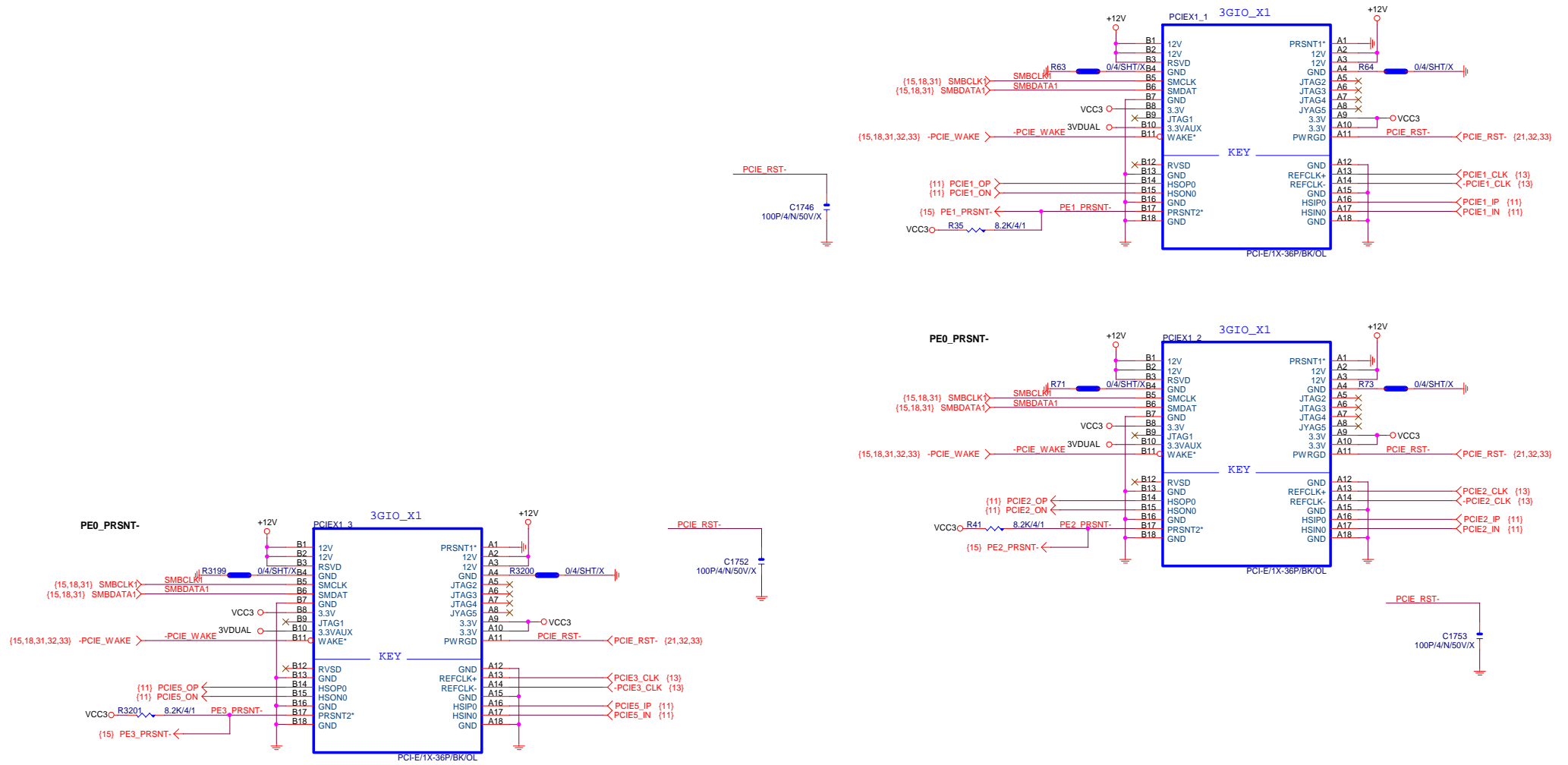
Title			
ATI SB700 SATA/IDE/HWM/SPI			
Size	Document Number		Rev
Custom	GA-970A-DS3P		1.0
Date:	Friday, May 10, 2013	Sheet	16 of 33

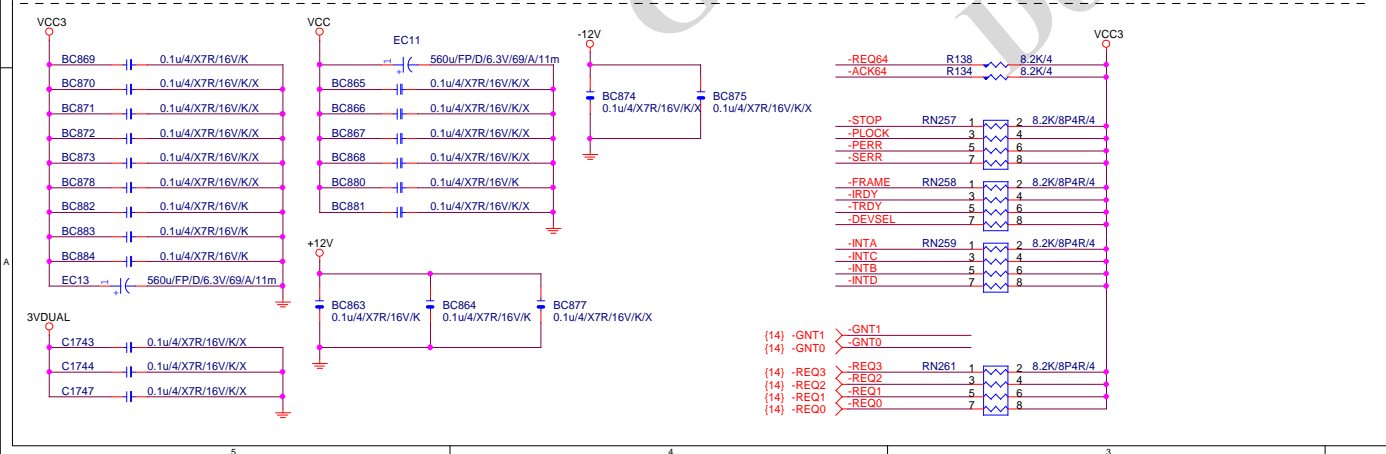


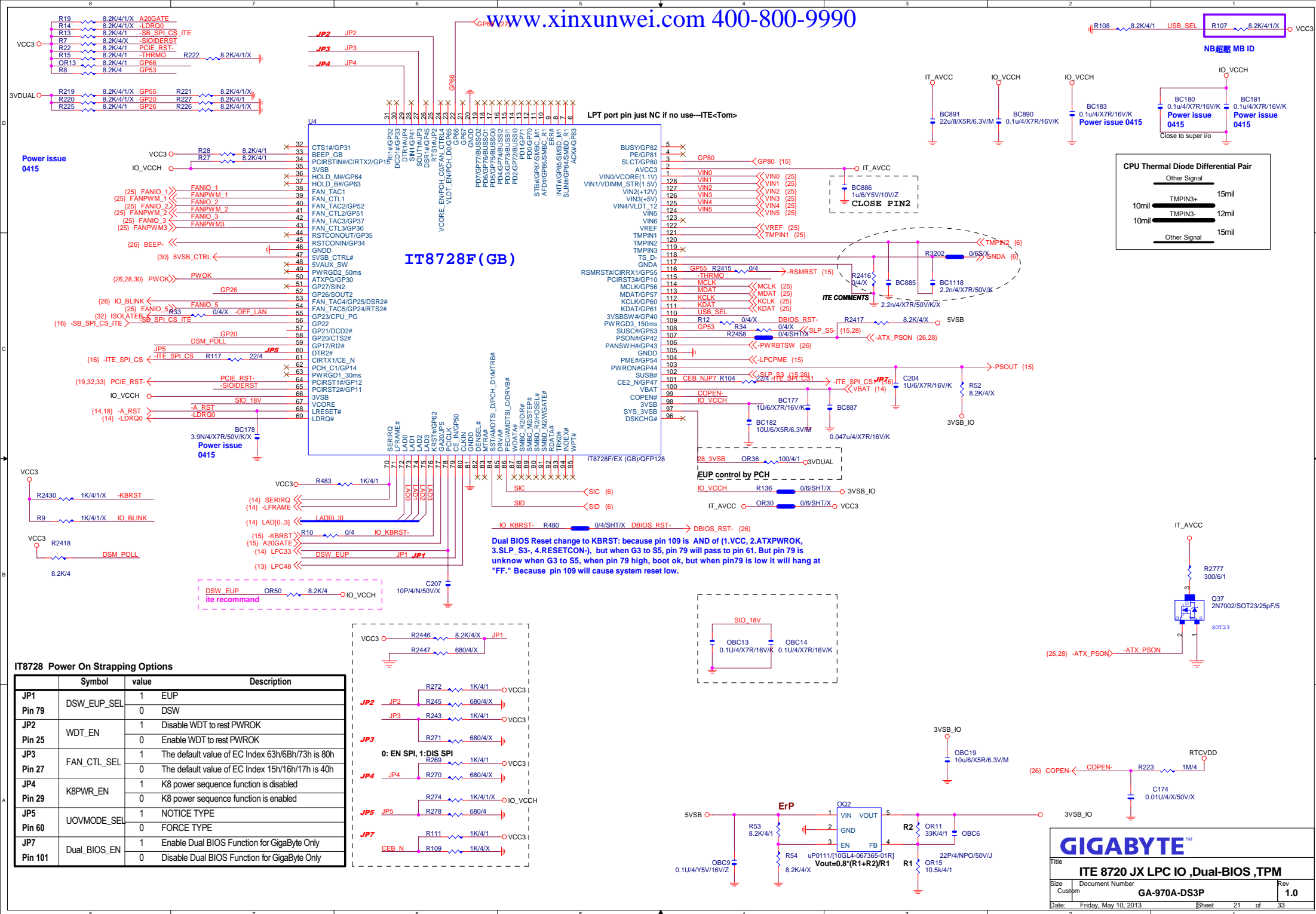
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.





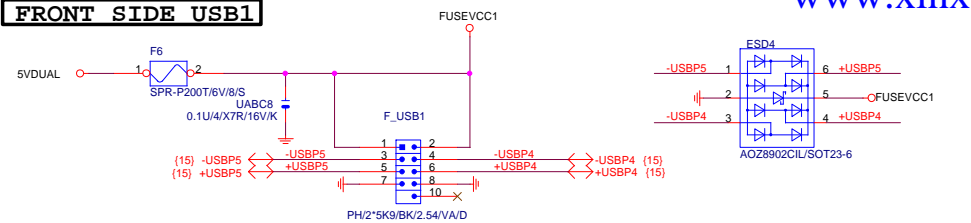




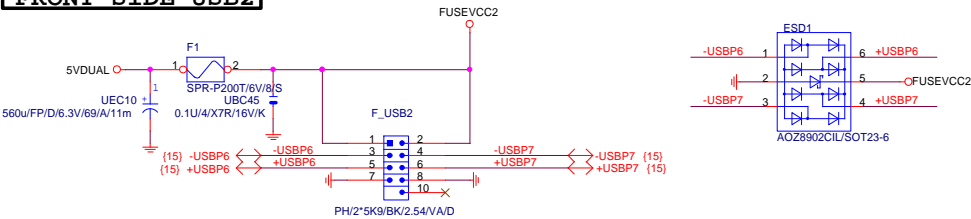


	Symbol	value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin 79		0	DSW
JP2	WDT_EN	1	Disable WDT to rest PWROK
Pin 25		0	Enable WDT to rest PWROK
JP3	FAN_CTL_SEL	1	The default value of EC Index 63h/6Bh/73h is 80h
Pin 27		0	The default value of EC Index 15h/16h/17h is 40h
JP4	K8PWR_EN	1	K8 power sequence function is disabled
Pin 29		0	K8 power sequence function is enabled
JP5	UOVMODE_SEL	1	NOTICE TYPE
Pin 60		0	FORCE TYPE
JP7	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
Pin 101		0	Disable Dual BIOS Function for GigaByte Only

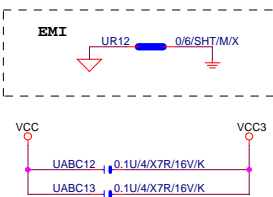
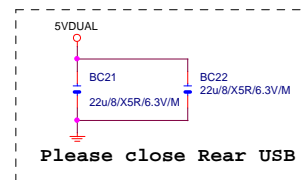
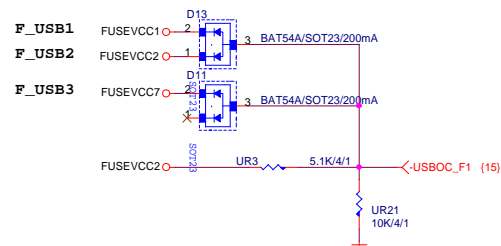
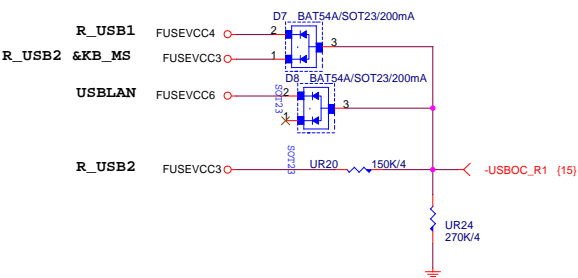
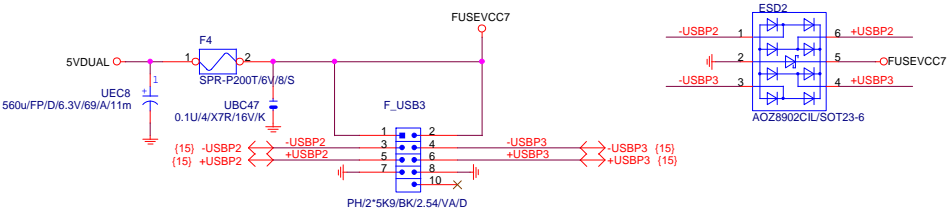
FRONT SIDE USB1



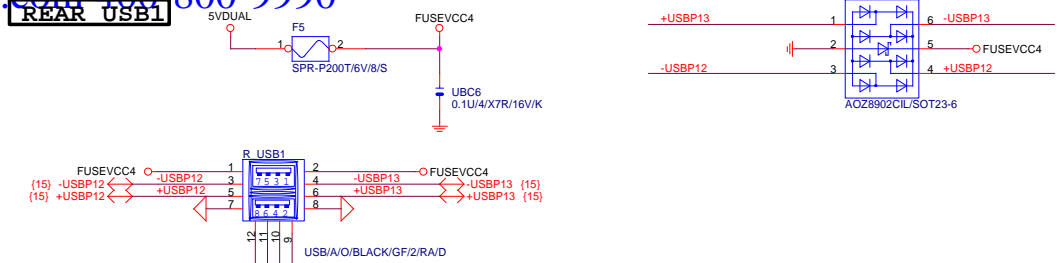
FRONT SIDE USB2



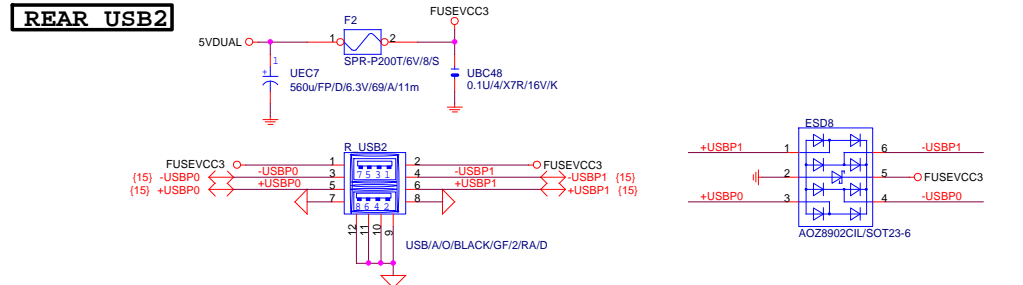
FRONT SIDE USB3



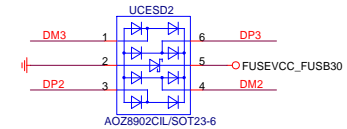
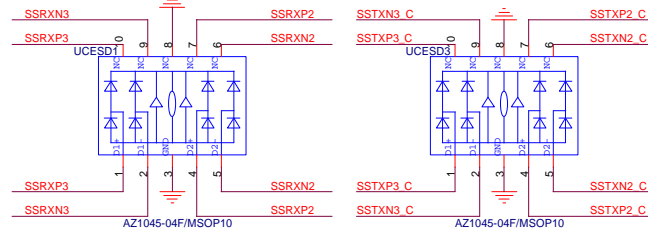
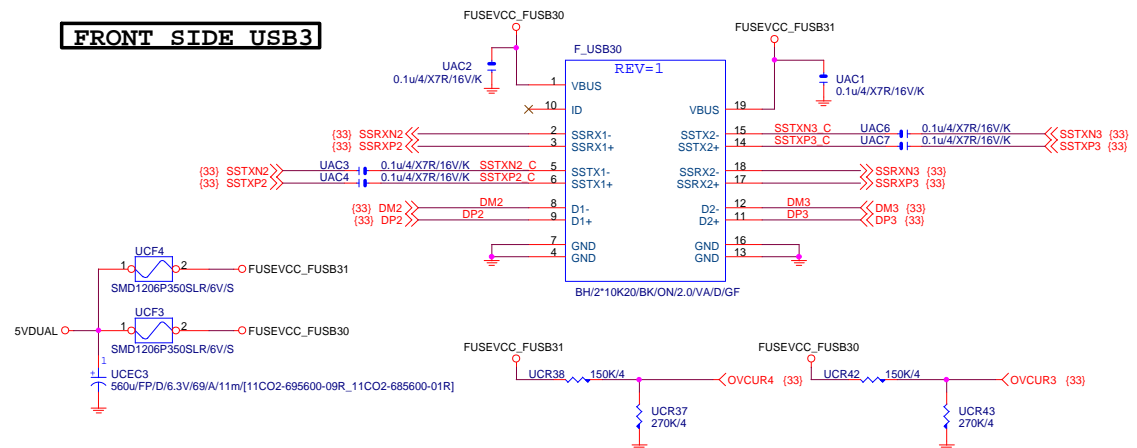
REAR USB1



REAR USB2



FRONT SIDE USB3



Close to connector

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For 892 with LDO

892W LDO

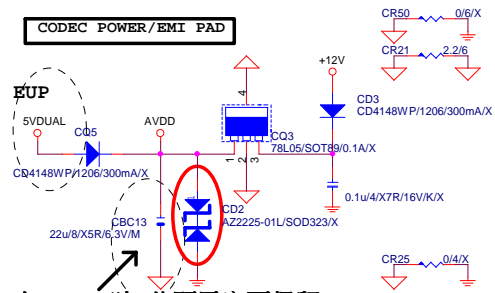
CBC7
22uF/8V5R/6.3V/M

CR51
0.1

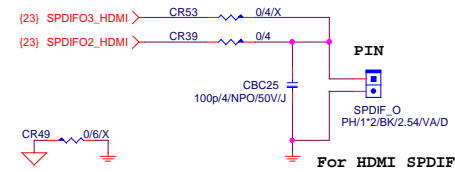
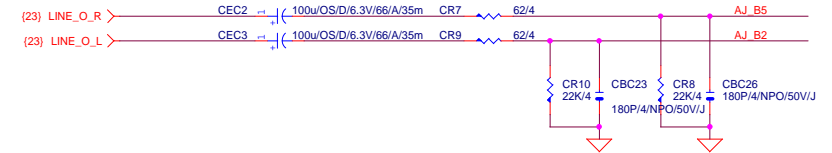
CD1
AZ2225-01L/SOD323

C5VDUAL

CODEC POWER/EMI PAD



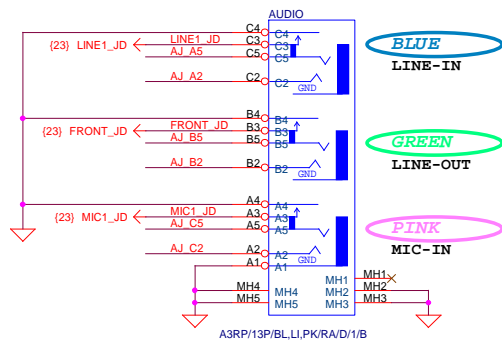
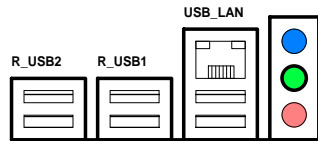
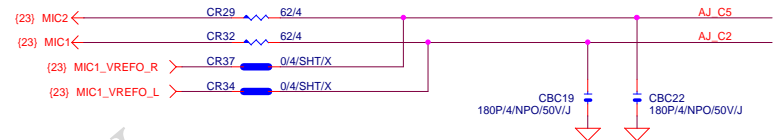
SPDIF

LINE OUT
FRONT OUT

LINE-IN



MIC

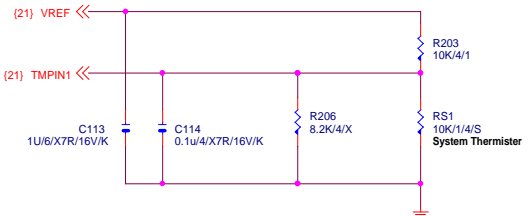


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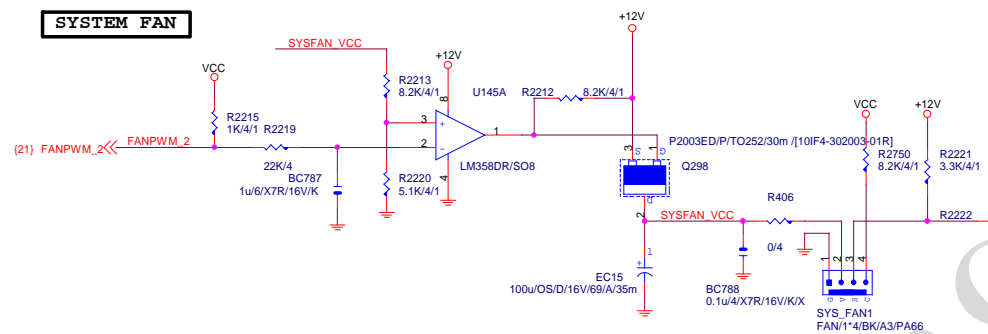
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AUDIO JACKSize
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GA-970A-DS3PRev
1.0

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Hardware Monitor circuits

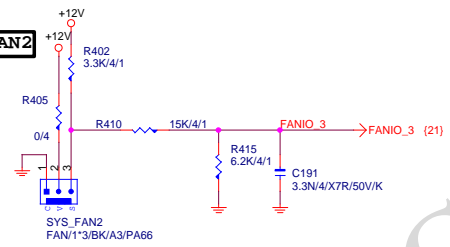


SYSTEM FAN

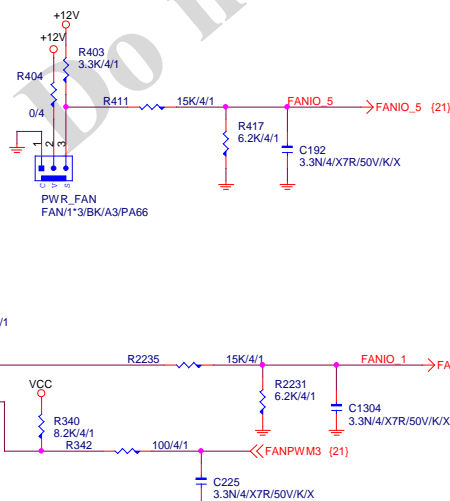
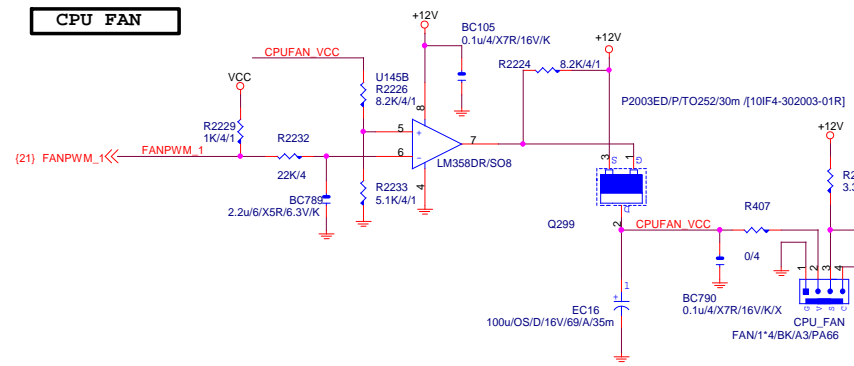


POWER FAN

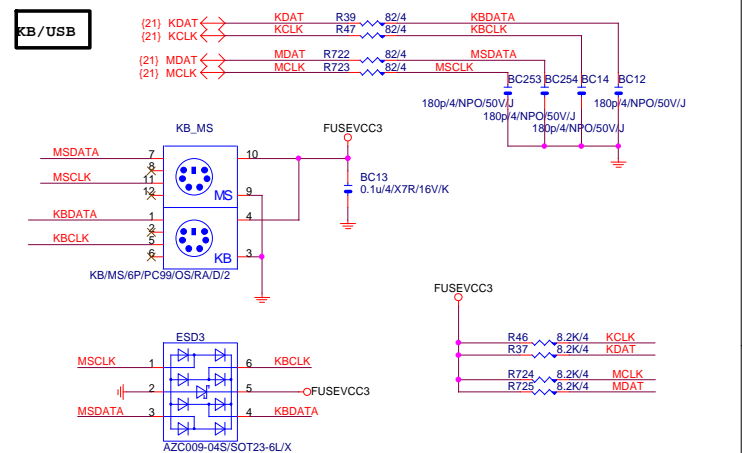
SYSTEM FAN2



CPU FAN



KB/USB



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FAN/HWMO KB/MS

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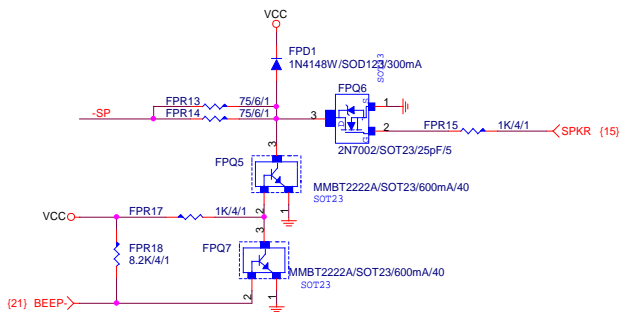
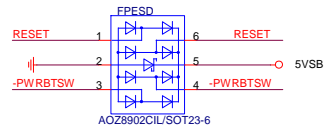
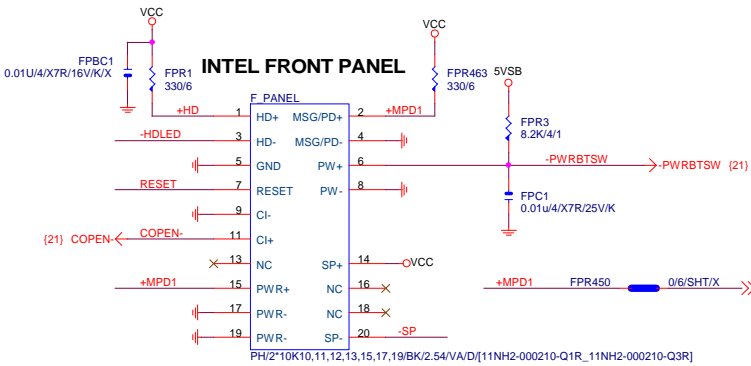
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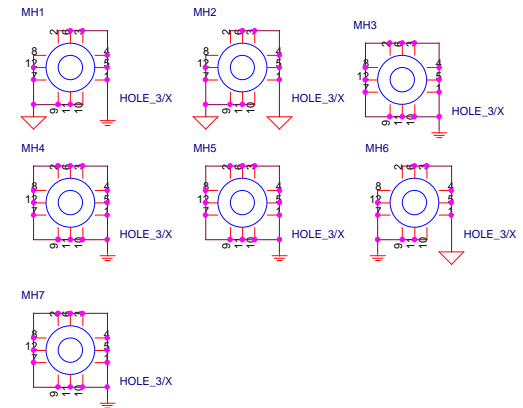
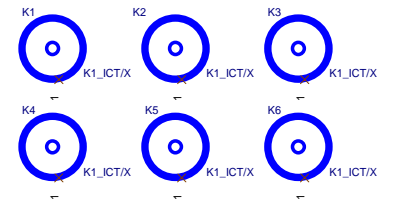
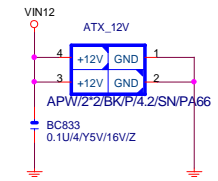
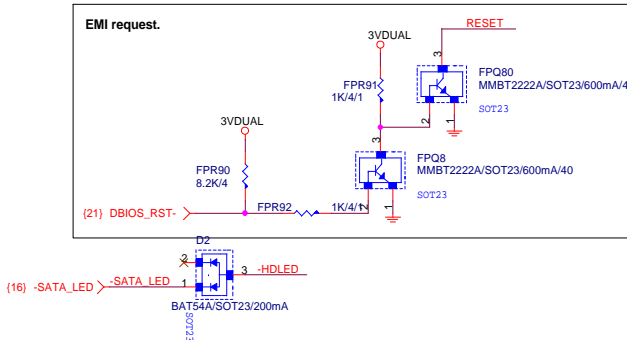
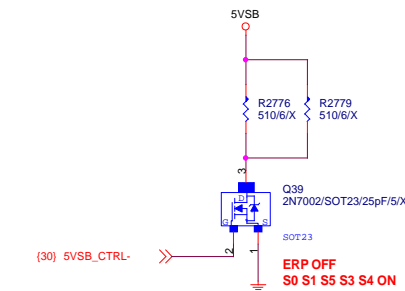
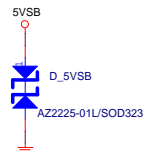
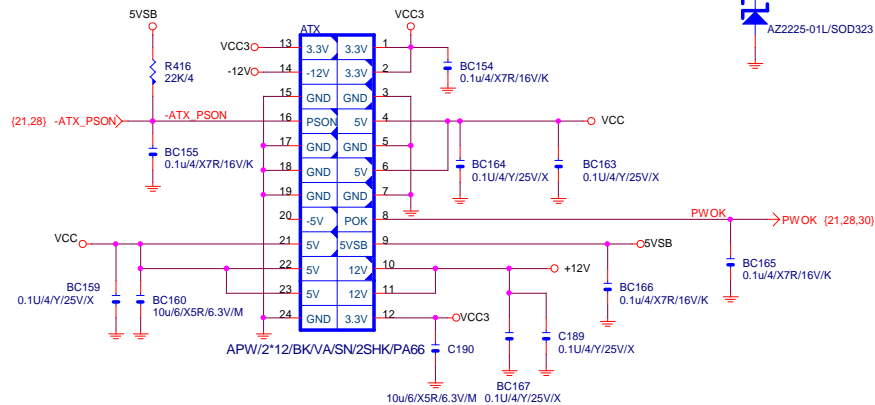
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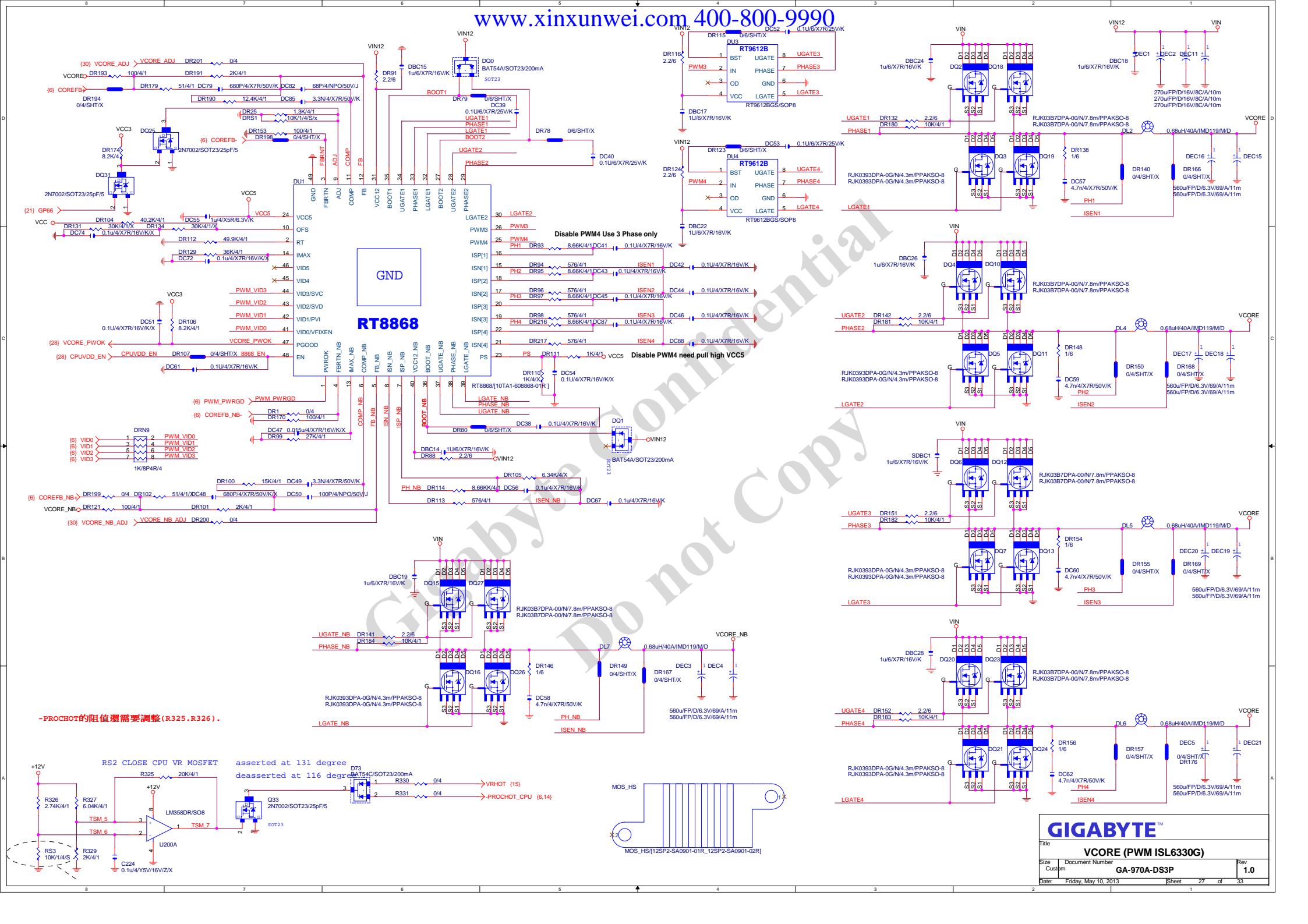
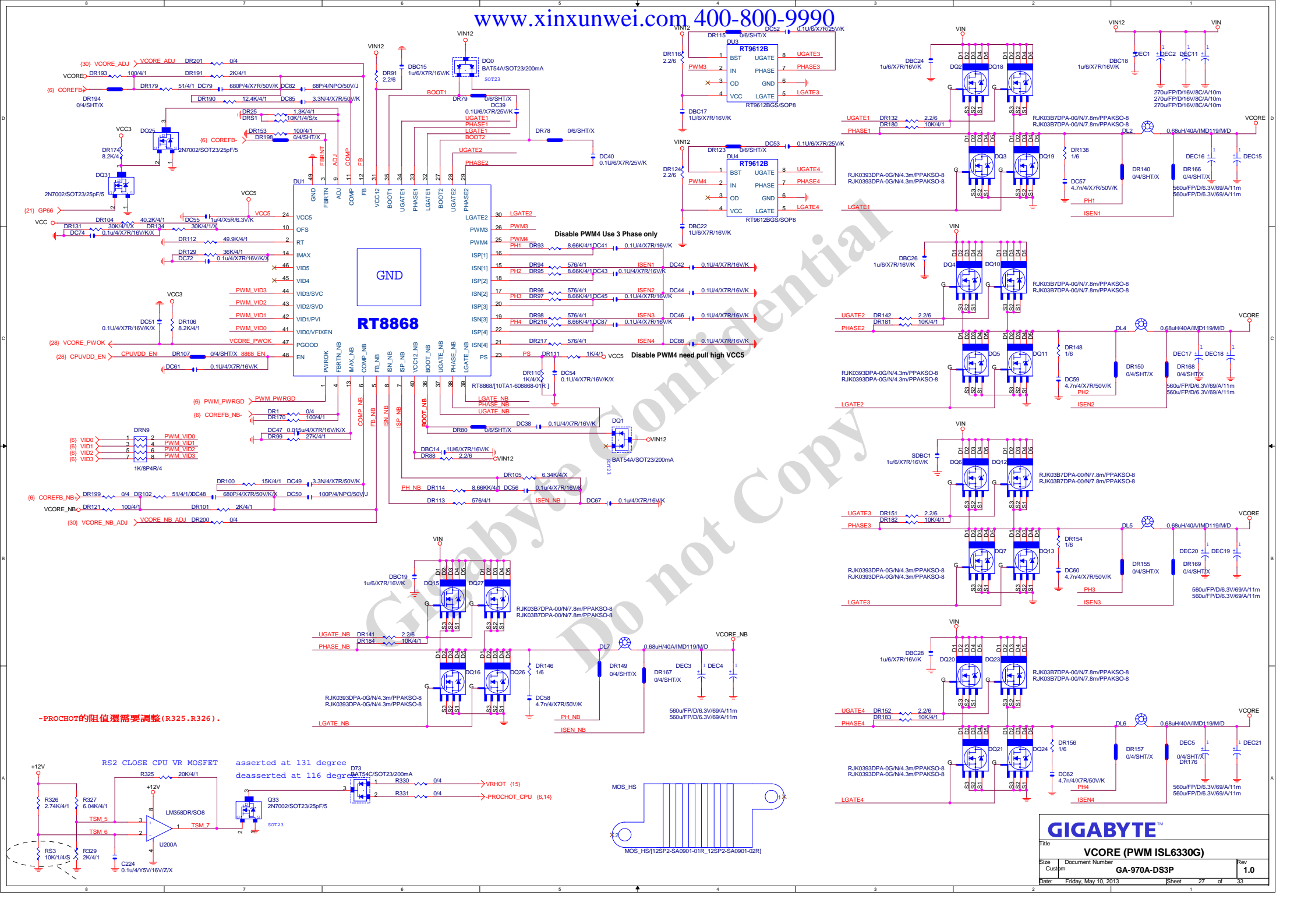
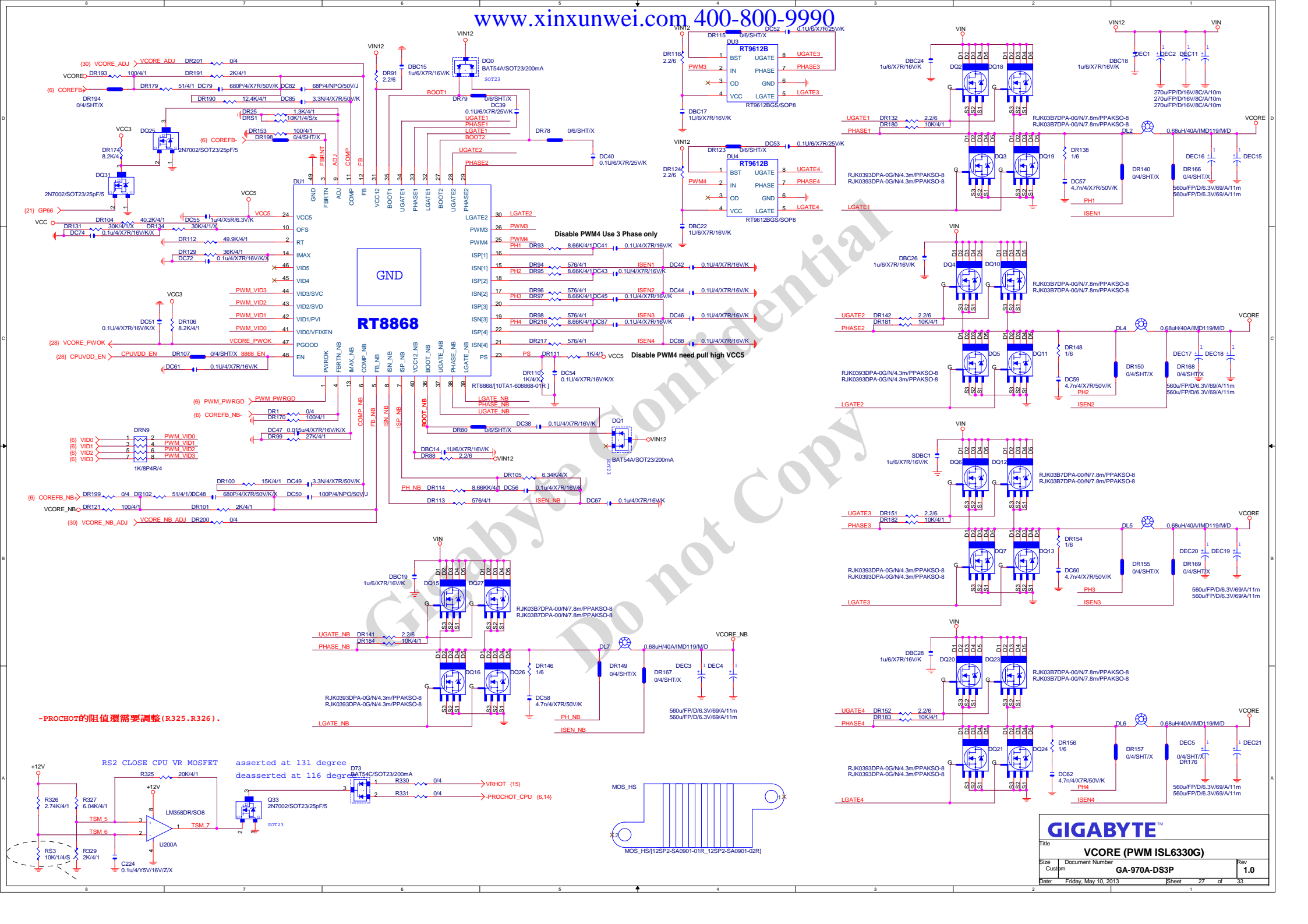
of

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ATX POWER CONNECTOR



[illegible]

www.xinxunwei.com 400-800-9990

RT8868

Disable PWM4 Use 3 Phase only

Disable PWM4 need pull high VCC5

PROCHOT的阻值還需要調整(R325.R326)。

asserted at 131 degree
deasserted at 116 degree

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Title: VCore (PWM ISL6330G)

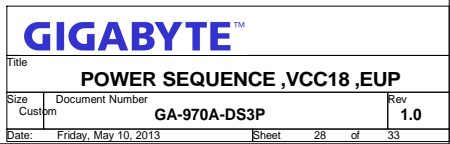
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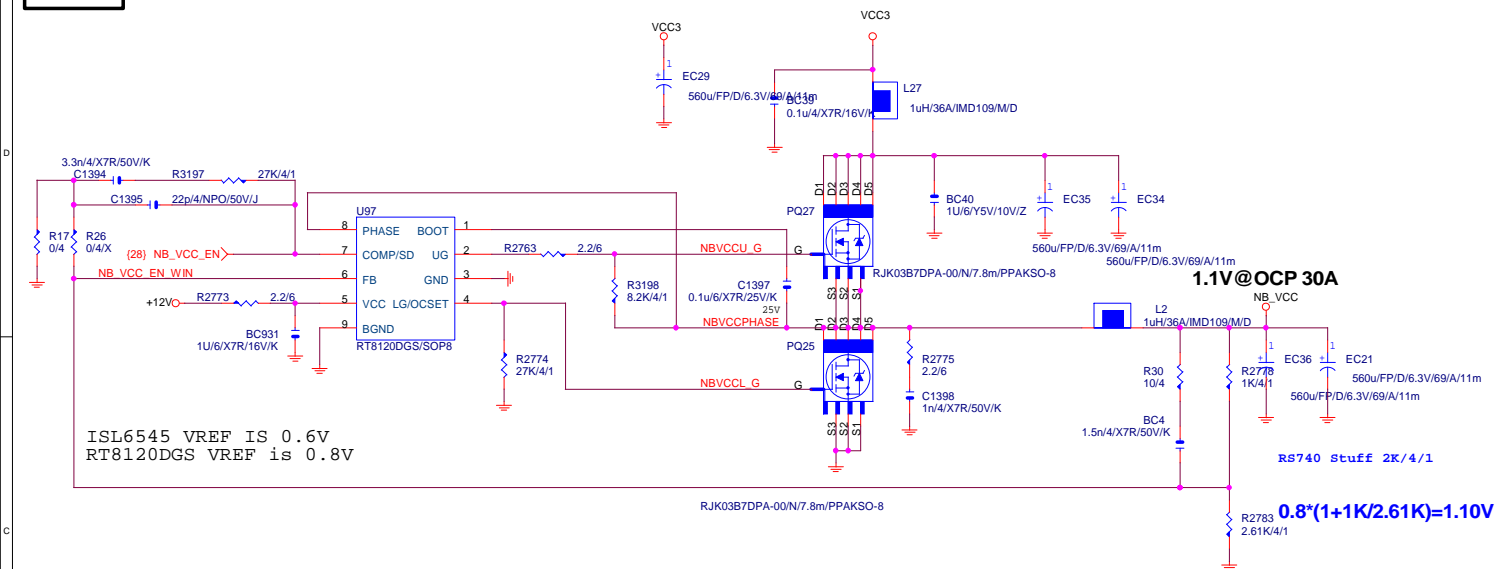
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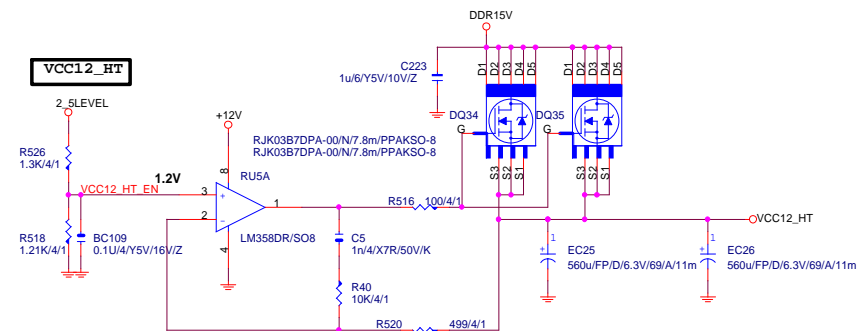
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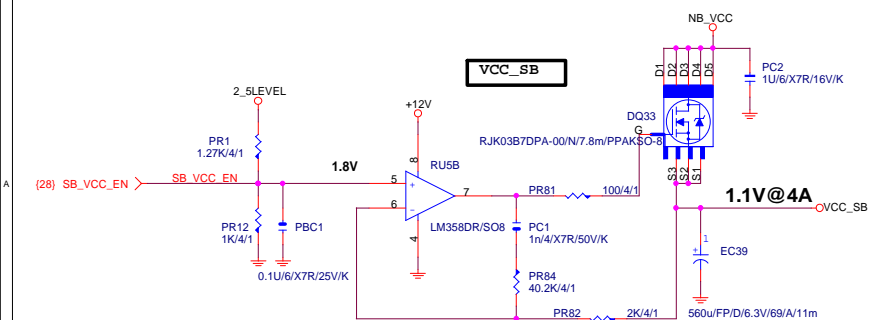
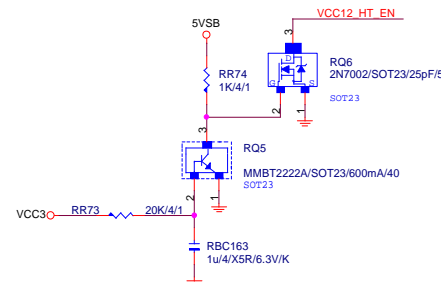
VCC_NB



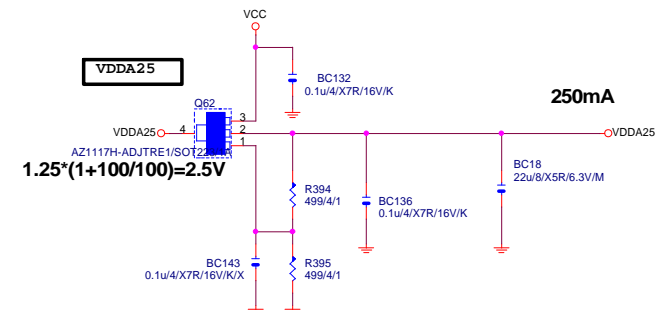
VCC12_HT



VCC_SB

Patch AMD Validation
VDDA25 & VCC12_HT
power sequence

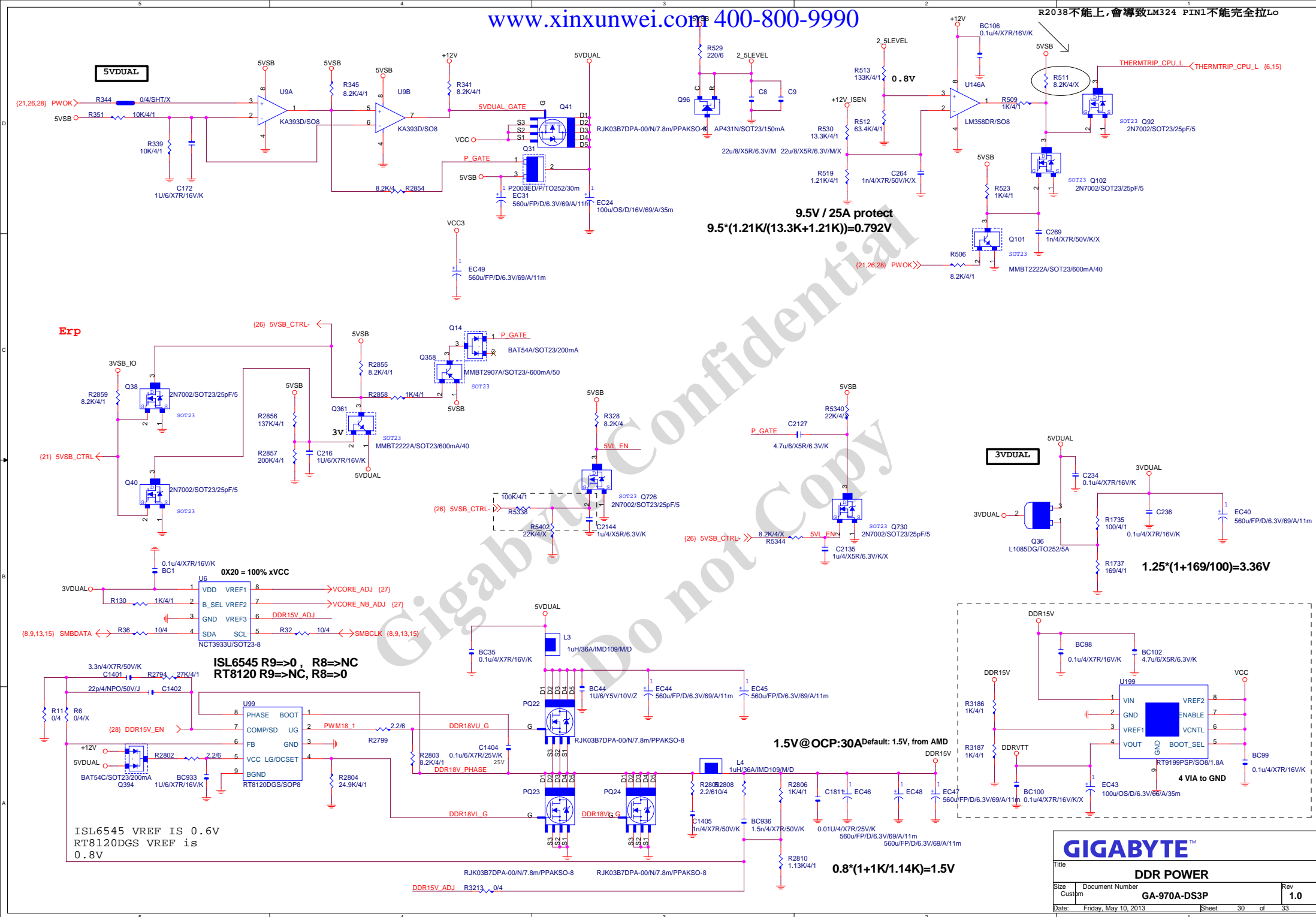
VDDA25

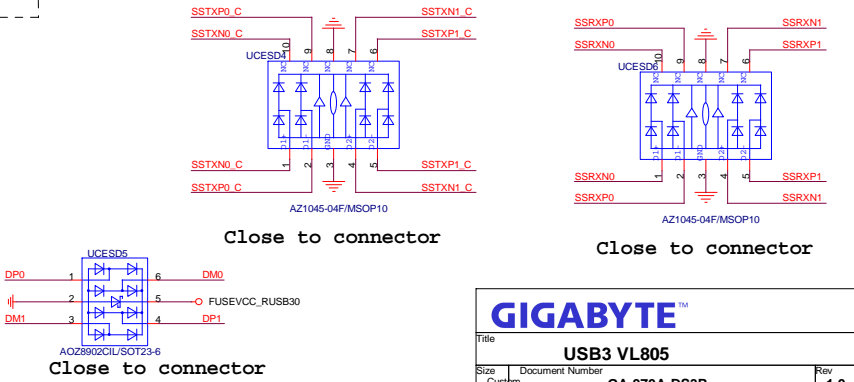
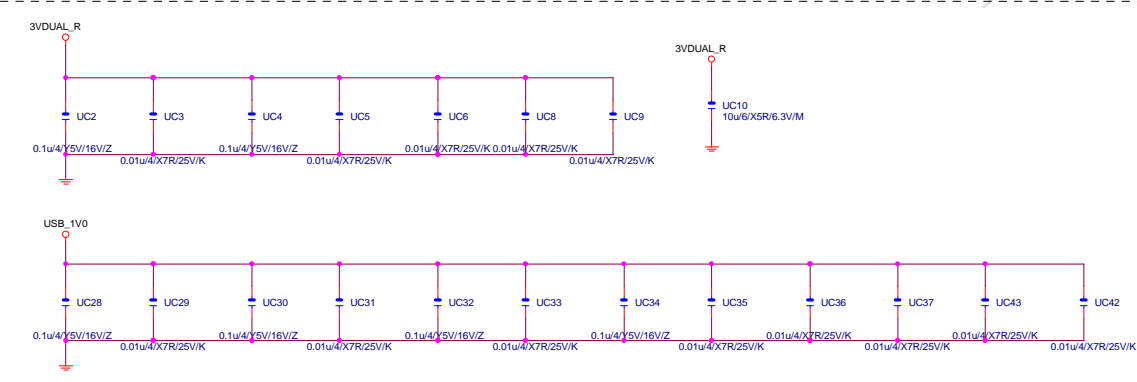
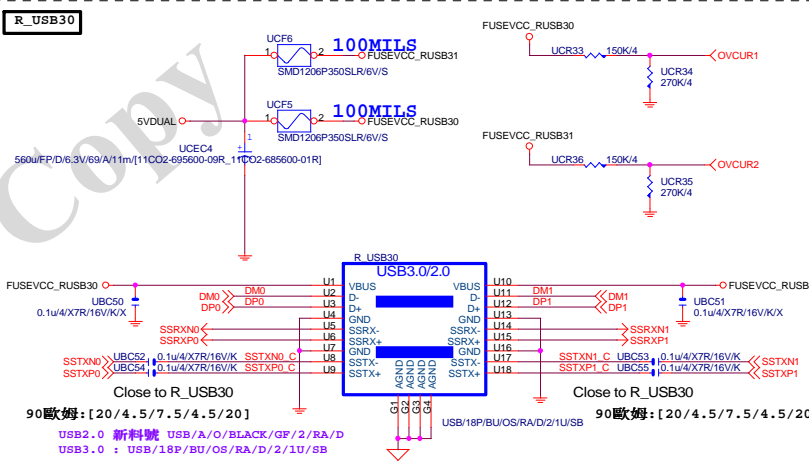
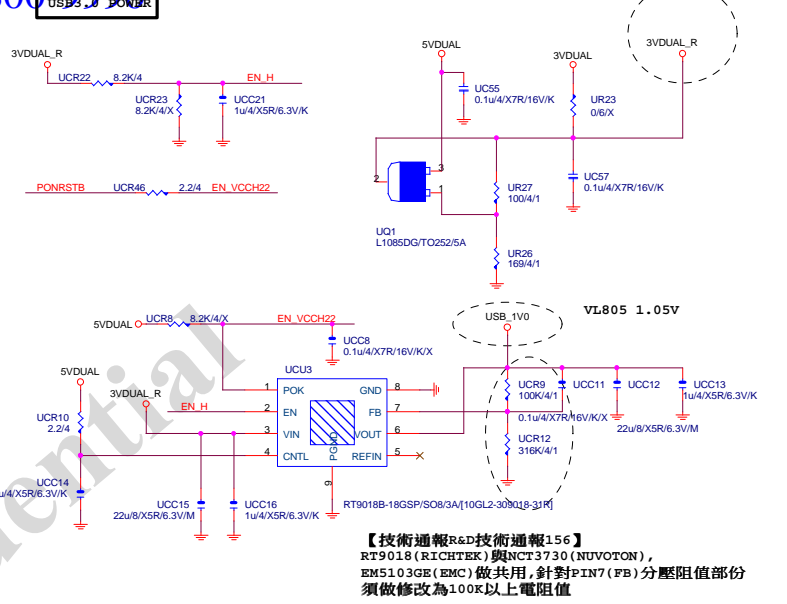
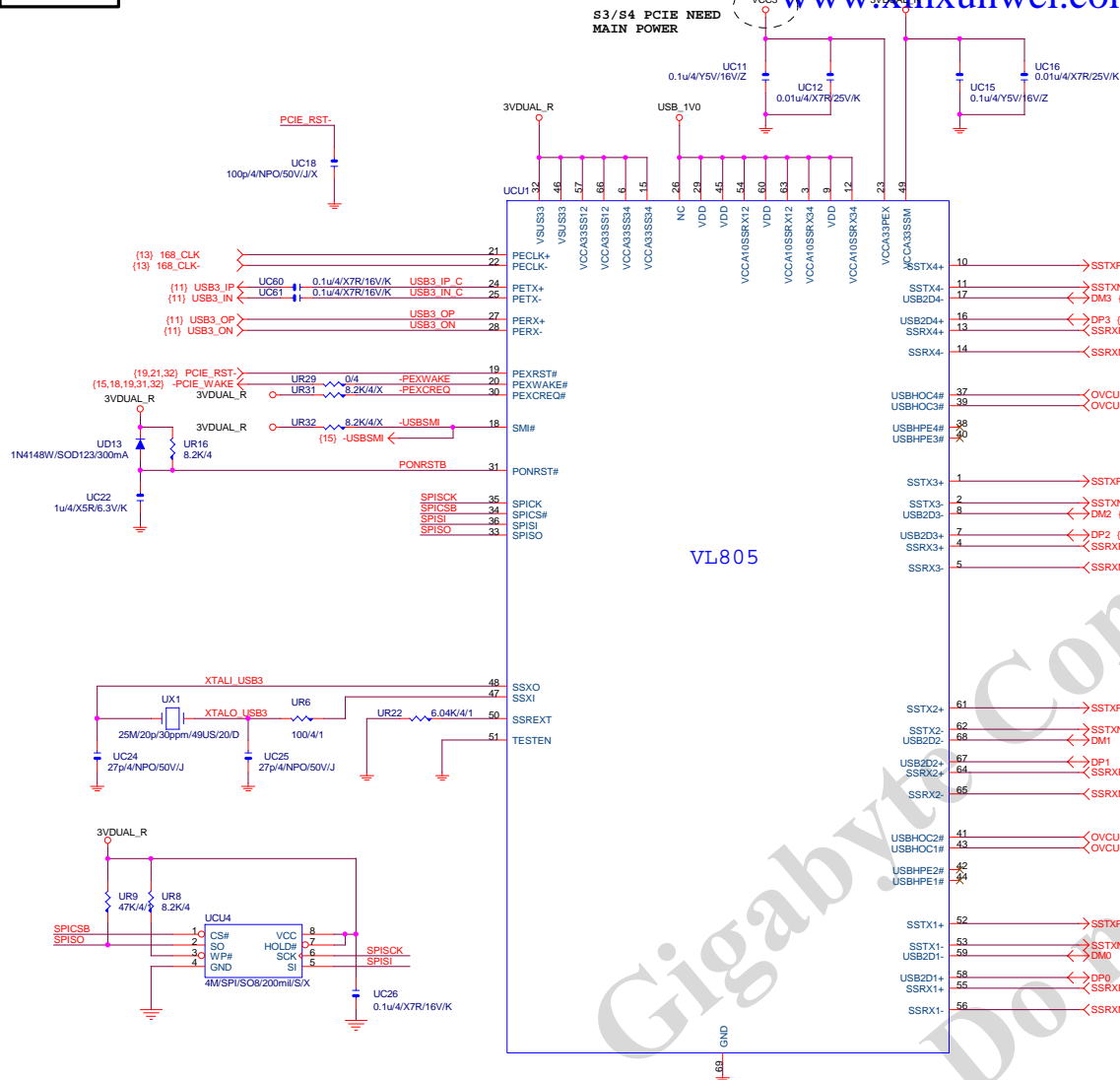


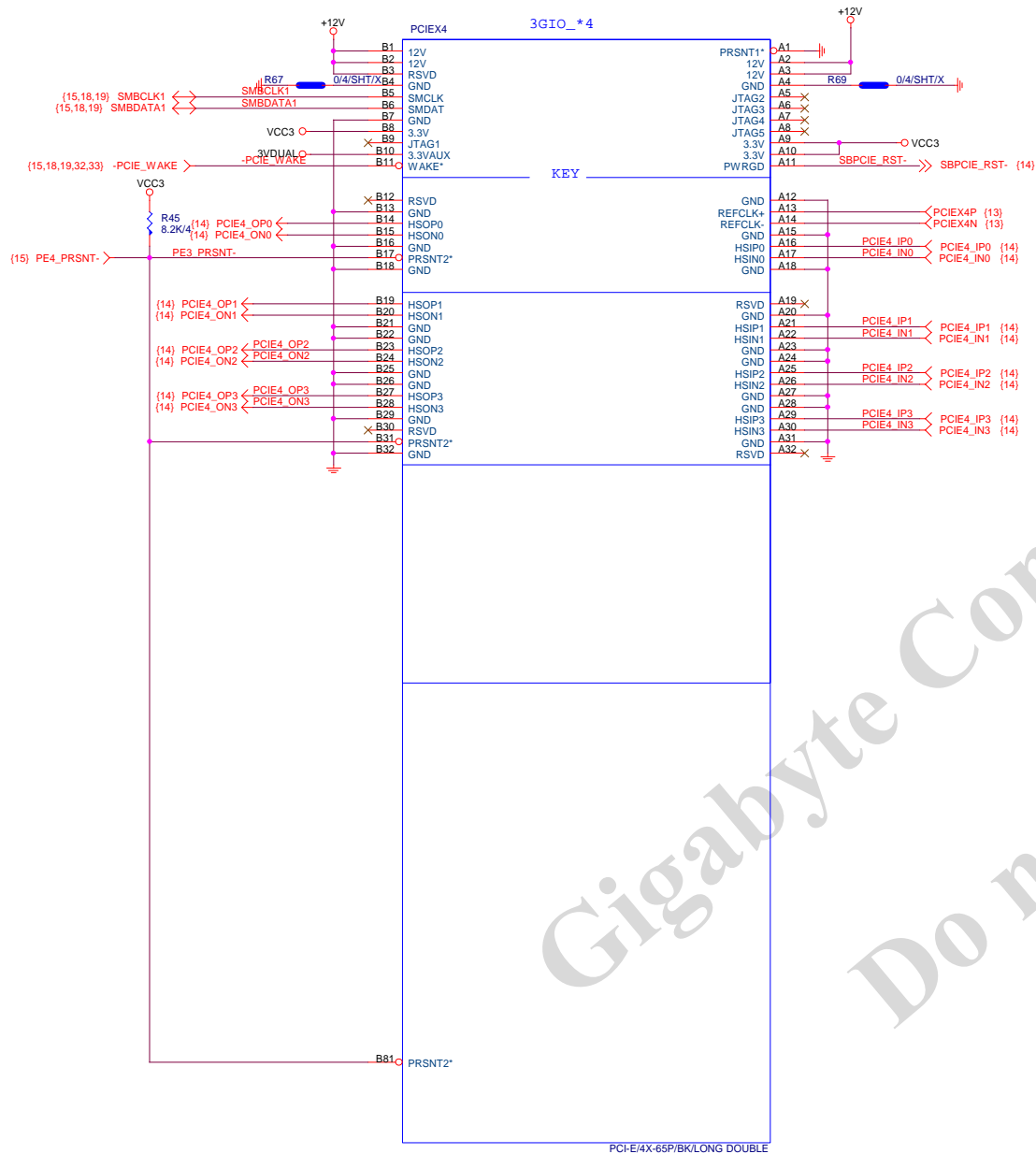
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NB/SB POWER, VCC12HT, VDDA25, VCC12DualSize
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Date:

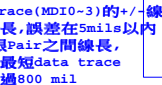
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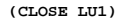
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要用1% 的電阻,trace不能太長,建議在200 mil以內



Pin34/35(VDDREG) 接到3VDUAL
的trace 建議寬度大於 40mil



RTL8101E:LR38/LC5/LR43/LC6-->0

RTL8111C:LC6-->0

RTL8102E:LC5/LC6-->0



```
RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
```

```
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1
```



Title	REALTK RTL8111C
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